Power Performance at 40 GHz of AlGaN/GaN High-Electron Mobility Transistors Grown by Molecular Beam Epitaxy on Si(111) Substrate

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Abstract—This letter reports on the demonstration of microwave power performance at 40 GHz on AlGaN/GaN high-electron mobility transistor grown on silicon (111) substrate by molecular beam epitaxy. A maximum dc current density of 1.1 $A \cdot mm^{-1}$ and a peak extrinsic transconductance of 374 $mS \cdot mm^{-1}$ are obtained for 75-nm gate length device. At $V_{DS} = 25$ V, continuous-wave output power density of 2.7 $W \cdot mm^{-1}$ is achieved at 40 GHz associated with 12.5% power-added efficiency and a linear power gain (G_p) of 6.5 dB. The device exhibits an intrinsic current gain cutoff frequency F_T of 116 GHz and a maximum oscillation frequency F_{MAX} of 150 GHz. This performance demonstrates the capability of low cost microwave power devices up to Ka-band.

Index Terms—AlGaN/GaN, high electron mobility transistor (HEMT), Ka-band, millimeter-wave power density.

I. Introduction

GALLIUM Nitride (GaN) High Electron Mobility Transistors (HEMTs) have emerged as the best candidate for high temperature, high voltage and high power operation in microwave and millimeter-wave ranges [1]. As regards to the fabrication of GaN HEMTs, silicon substrate offers an interesting alternative to silicon carbide (SiC) substrate through its low cost, large area availability, and possibility to process and integrate MOS technology [2]. GaN growth on silicon (Si) substrates has received a lot of attention by the most relevant laboratories, permitting to obtain good material quality and electrical properties for AlGaN/GaN HEMTs epi-material on Si(111) substrate for applications up to millimeter wave range [3]. Regarding state of the art at 40 GHz on Si(111), Bolognesi *et al.* obtained 2.05 W.mm^{-1} with

an AlGaN barrier [4] while Medjdoub *et al.* demonstrated 2.5 W.mm^{-1} with an AlN barrier [5] both grown by metal-organic chemical vapor deposition (MOCVD). Alternatively, Soltani *et al.* have demonstrated a record output power density of 3.3 W.mm^{-1} at 40 GHz with an AlGaN barrier grown by MBE on Si(110) orientation [6]. Compared with MBE, nucleation of III-N material on silicon substrate and in particular the AlN/Si interface is more difficult to monitor with MOCVD. This is due to higher growth temperature and interface quality having a drastic influence on the films structural quality [7]. Furthermore, the possible diffusion of doping species from (Si) towards (Al, Ga) involves consequences on electrical traps and/or RF losses. At last, due to the growth temperature, the risk of AlGaN barrier strain relaxation is lower with MBE [8]. Consequently, there are still benefits from using AlGaN/GaN material system grown by MBE, compared with other barrier materials such as InAlN and AlN. In this letter, strong efforts were preliminary directed towards the growth of an optimized epitaxial structure in terms of sheet resistance while keeping a thin AlGaN barrier [9]. As a result, the proposed heterostructure yields a sheet resistance as low as 250 Ω/□ through a combination of very high sheet carrier density and high mobility. Furthermore, lag effects are limited thanks to optimized surface passivation process. The fabrication of transistors featuring sub-100 nm gate-length enables to achieve current gain cut-off frequencies beyond 100 GHz. In this letter, DC, RF, pulsed and large signal measurements are reported for AlGaN/GaN HEMT grown on standard high-resistivity Si(111) substrate by ammonia source MBE with 75 nm T-shaped gate. The capability of AlGaN/GaN transistors on Si(111) substrate is demonstrated for high frequency microwave power applications at 40 GHz with a continuous wave output power density of 2.7 W.mm^{-1} associated with a power added efficiency of 12.5 % corresponding to the highest saturated power density ever reported on Si(111) substrate to date.

II. Material Growth and Device Technology

AlGaN/GaN heterostructure was grown on a high-resistivity phosphorus doped silicon (111) substrate ($\rho > 3$ kΩ.cm) by ammonia source MBE. The epitaxial structure consists of a 10-nm-thick $Al_{0.29}Ga_{0.71}N$ barrier capped with 0.5-nm-thick GaN layer. A 1-nm-thick AlN exclusion layer is used to
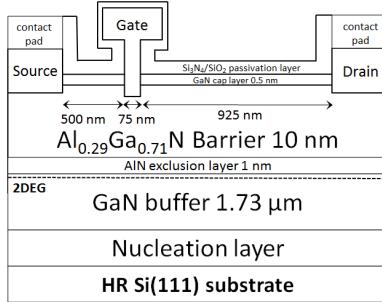
Fig. 1.   Cross section of the fabricated AlGaN/GaN-on-Si(111) HEMT.

Fig. 2. $I_{DS}(V_{DS})$, DC and pulse characteristics for different quiescent bias points for $2 \times 50 \times 0.075$ μm^2 AlGaN/GaN HEMT on Si(111) substrate. Inset represents $g_m(V_{GS})$ and transfer characteristics at $V_{DS} = 6$ V.

reduce alloy scattering and improve carrier confinement within the 2D electron gas (2DEG). The buffer consists of a 1.73-μm-thick GaN associated with AlN/$Al_{0.15}Ga_{0.85}$N stress mitigating layers (Fig. 1). The crystal quality is assessed through the full width at half maximum (FWHM) of the GaN (002) and (302) omega scan X-ray diffraction (XRD) leading to 730 arcsec and 1800 arcsec respectively. The (302) XRD peak width is correlated with the threading dislocation density (TDD). According to calibration curves based on dislocation counting using atomic force microscopy (AFM) and plane view transmission electron microscopy (TEM), the measured (302) FWHM leads to a TDD of $5 \times 10^9 cm^{-2}$. Lower TDDs of 1-$2 \times 10^9 cm^{-2}$ have already been reported with 2-3.4-μm-thick HEMT compatible buffer layers grown by MOCVD [10], [11]. Nevertheless, a degradation of the buffer isolation properties with the enhancement of the crystal quality was observed [10]. Hence, the present buffer is a trade-off between crystal quality and buffer isolation. The device fabrication starts with Ti/Al/Ni/Au ohmic contacts deposited by e-beam evaporation. This is followed by rapid thermal annealing (RTA) at 850°C for 30 s. Devices are isolated by N^+ ion multiple implantations. Device under test (DUT) in this letter features a two-finger configuration with $L_g = 75$ nm, $W = 2 \times 50$ μm and $L_{SD} = 1.5$ μm. T-shape gates are patterned by electron-beam lithography process using optimized (PMMA/COPO/PMMA) tri-layer resist stack. Schottky gate metal stack consists of evaporated Ni/Au (40/300 nm). This step is followed by a N_2O pretreatment for two minutes and a passivation based on Si_3N_4/SiO_2 (50/100 nm) bilayer dielectric performed by plasma-enhanced chemical vapor deposition (PECVD) at 340°C leading to mitigation of the surface states activity. Finally, the thick interconnection is processed by Ti/Au overlay metallization. Transmission line modeling (TLM) data reveal a contact resistance R_C of 0.29 Ω.mm. After passivation, this structure provides a sheet carrier density n_S of $1.28 \times 10^{13} cm^{-2}$ associated with a high electron mobility of 1930 $cm^2/V.s$ leading to a low sheet resistance R_{SH} of 250 $\Omega/\square$ obtained from Hall measurement.

III. RESULTS AND DISCUSSIONS

A. DC Characteristics

Fig. 2 shows pulsed and DC measurements including $g_{m,ext}(V_{GS})$ and transfer characteristics in the inset for a $2 \times 50 \times 0.075$ μm^2 device. A maximum DC current
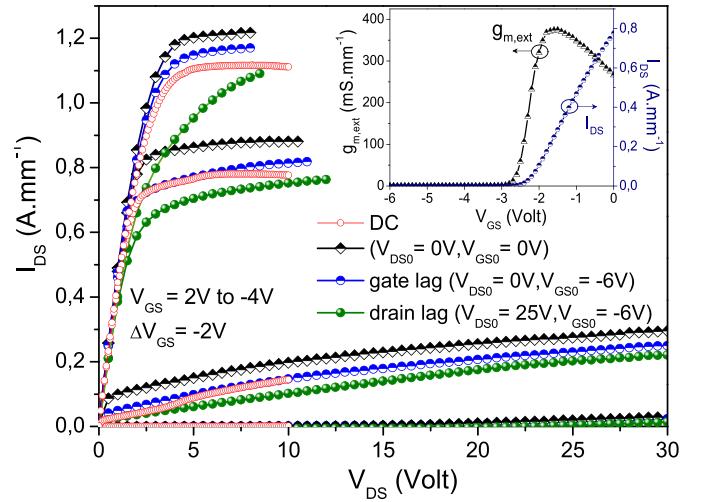
density $I_{DS,max}$ of 1.1 A.mm^{-1} is obtained at $V_{GS} = 2$ V. Extrinsic transconductance $g_{m,ext}$ beyond 350 mS.mm^{-1} is obtained for different V_{DS} from 4 V to 25 V with a peak transconductance of 374 mS.mm^{-1} at $V_{GS} = -1.6$ V and $V_{DS} = 6$ V. Source and drain access resistances R_S and R_D of 5.7 Ω and 6.8 Ω respectively are extracted using small-signal cold-FET analysis. Hence, it becomes possible to deduce an associated intrinsic transconductance $g_{m,int}$ of 475 mS.mm^{-1}. A threshold voltage V_{th} of -2.3 V is deduced from transfer characteristic at $V_{DS} = 6$ V and the three-terminal breakdown voltage determined at pinch-off is BV = 55 V. The I_{ON}/I_{OFF} ratio reaches 10^4 and remains inherently limited by the leaky behavior of the gate. Improvement will be brought in the future to mitigate this effect to keep high I_{ON}/I_{OFF} ratio and near constant pinch-off value all over the V_{DS} range.

B. Pulse Measurement

Pulse measurement is carried out using different quiescent bias points (V_{DS0}, V_{GS0}) with a setup featuring 500 ns pulse duration with 0.3 % duty cycle. Fig. 2 shows the pulsed I-V characteristics for different quiescent bias points and enables to estimate lag phenomena. At the quiescent bias point ($V_{DS0} = 0$ V, $V_{GS0} = 0$ V), thermal and trapping effects are both suppressed and the associated curves act as a reference to quantify gate and drain lag effects. A current drop as low as 4 % is observed under gate lag condition ($V_{DS0} = 0$ V, $V_{GS0} = -6$ V). Regarding drain lag effect ($V_{DS0} = 25$ V, $V_{GS0} = -6$ V), a current drop of 20 % is observed from a comparison with the maximum current density at ($V_{DS0} = 0$ V, $V_{GS0} = 0$ V). As exposed, there are still possibilities to improve the DC-to-RF dispersion, e.g. using either in-situ SiN passivation layer or more adequate plasma pre-treatment.

C. RF Characteristics

Scattering parameters S_{ij} are measured from 0.25 to 67 GHz using Vector Network Analyzer (VNA) and off-wafer
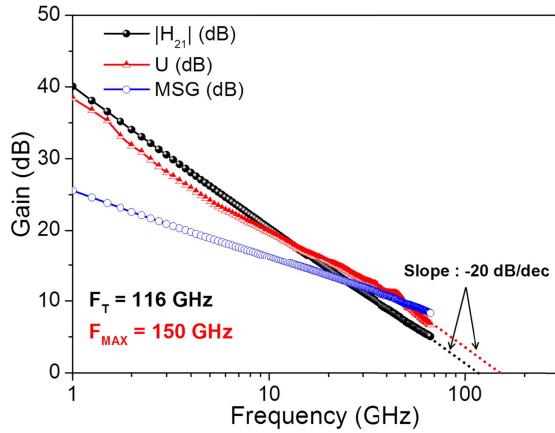
Fig. 3. Current gain modulus $|H_{21}|$, Mason's unilateral gain (U) and Maximum Stable Gain (MSG) versus frequency, for a $2 \times 50 \times 0.075$ μm^2 AlGaN/GaN HEMT on Si(111) substrate at $V_{GS} = -1.6$ V and $V_{DS} = 6$ V.
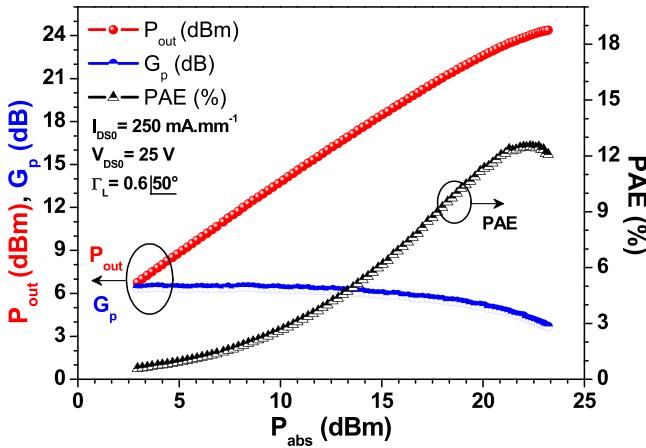

Fig. 4. Output power, power gain and power added efficiency versus absorbed power at 40 GHz for a $2 \times 50 \times 0.075$ μm^2 AlGaN/GaN HEMT on Si(111) substrate at $V_{DS} = 25$ V.

Line-Reflect-Reflect-Match (LRRM) calibration. Current gain modulus ($|H_{21}|$) and Mason's unilateral gain (U) are deduced from S_{ij} parameters versus frequency. The contributions associated with PADs (i.e. capacitive and inductive components) are de-embedded using the two-steps technique on dedicated open-short dummy devices. At $V_{DS} = 6$ V and $V_{GS} = -1.6$ V, corresponding to the peak of extrinsic transconductance, an intrinsic current gain cut-off frequency F_T of 116 GHz associated with a maximum oscillation frequency F_{MAX} of 150 GHz are achieved through the linear -20 dB/decade extrapolation of the measurement (Fig. 3). Good F_{MAX}/F_T ratio is intrinsically linked with the technological maturity. Indeed, T-shape-gate makes it possible to reduce the gate resistance (R_g), while a high transconductance/output conductance ratio g_m/g_d of 12 is obtained from small-signal modeling through the combination of short gate length and thin barrier (10 nm).

D. Microwave Power Measurement

Large-signal microwave power measurement at 40 GHz is performed using an active load-pull setup under CW conditions with a large-signal network analyzer (LSNA) working

up to 50 GHz. At $V_{DS} = 20$ V and $I_{DS} = 250$ mA.mm^{-1} corresponding to AB class operation, selected devices show good microwave power performance. The optimal load impedance is $\Gamma_{load} = 0.6\angle 50°$. In these conditions, devices exhibit a linear power gain (G_p) of 7 dB and a saturated output power density (P_{out}) of 2.55 W.mm^{-1} associated with a power-added efficiency (PAE) of 14 %. Measurement was also carried out at $V_{DS} = 25$ V and $I_{DS} = 250$ mA.mm^{-1} using the same optimal load impedance. In this case (Fig. 4), a linear power gain (G_p) of 6.5 dB and a saturated output power density (P_{out}) of 2.7 W.mm^{-1} are obtained associated with a PAE of 12.5 %. This result is very promising and to our knowledge constitutes the large signal state of the art at 40 GHz for AlGaN/GaN HEMTs on Si(111) substrate.

IV. Conclusion

We have demonstrated high small-signal and RF power performances for a $2 \times 50 \times 0.075$ μm^2 Al$_{0.29}$Ga$_{0.71}$N/GaN HEMT on a (111) oriented silicon substrate. An output power density of 2.7 W.mm^{-1} is obtained associated with a PAE of 12.5 % and a linear power gain of 6.5 dB. These values indicate that GaN-based MBE technology still presents great potential to get good microwave power at high frequency. To our knowledge, this performance constitutes state of the art at 40 GHz for AlGaN/GaN HEMT on Si(111) substrate whatever the growth technique. Top heat spreader or substrate thinning constitute interesting solutions to minimize thermal effects due to the relatively low thermal dissipation of the silicons substrate.

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