Performance Limiting Leakage Current Across Ar-Implantation Isolation in AlGaN/GaN Structures for High Power Applications

Janina Moereke, Erwan Morvan, William Vandendaele, Fabienne Allain, Alphonse Torres, Matthew Charles and Marc Plissonnier

Univ Grenoble Alpes, F-38000 Grenoble, France
CEA, Leti, MINATEC Campus, F-38054 Grenoble, France
janina.moereke@cea.fr, Tel.: +33 (0) 4 387 84005

Keywords: Isolation, AlGaN/GaN, leakage current, electrical characterization, power devices

Abstract

Electrical characterization of AlGaN/GaN heterojunctions isolated by Ar-implantation identified three conduction regimes. These include an Ohmic regime below 100V associated with conduction across the implanted area itself as well as an exponential regime above 400V associated with a conduction across the buffer or buried interfaces with the substrate. While the extraction of activation energies found an average of roughly 0.85eV for the Ohmic regime, activation energies above 400V were consistent with a Poole-Frenkel conduction mechanism. Time-dependent measurements showed further a capacitive effect for conduction across the buffer at room temperature. Having identified the performance limiting conduction path through the buffer layers, these experimental results can also be used as a tool for epitaxy assessment very early on in the production process.

INTRODUCTION

GaN-based devices for high power conversion applications have been of great interest in recent years due to their promising performance at high temperatures and high breakdown voltages [1]. Device isolation plays a crucial part in exploiting the power capabilities of GaN by limiting leakage currents on the wafer. High electric fields, shown to be at the origin of degradation through trap generation [2], have also been identified as the driving mechanism for premature breakdown in isolation structures [3]. A comparison of mesa etch technology and isolation through ion implantation showed that the latter performs best for high voltage applications due to a reduction in peak electric field strength at the corner of the Ohmic contacts [2]. While the high electric fields produced during high power operation of an AlGaN/GaN HEMT are supported by the structure thanks to the wide bandgap of GaN, the lattice mismatch with Si, the most suitable substrate for high power applications [4], results in dislocations in the buffer layers. For a wide bandgap material such as GaN, defects can often result in deep trap levels that can reduce the device's performance due to trapping related phenomena such as current collapse and leakage currents [5,6]. Characterization of leakage currents vertically across AlGaN/GaN devices as well as test structures has shown results consistent with space-charge limited conduction [7,8], band-to-band tunneling [9,10] or Poole-Frenkel mechanisms [11, 12]. Previous characterization of leakage current across the device isolation have identified conduction paths making use of the buffer/substrate interface [11]. However, a detailed study identifying the contribution to leakage currents of both isolation technology as well as the quality of the epitaxy has not been presented so far. Consequently the performance limiting factor for high power applications has not been identified until now.

EXPERIMENTAL DETAILS

Test structures under investigation in this work were based on heterojunctions consisting of a 24 nm AlGaN barrier, a 100 nm unintentionally doped GaN channel and a carbon doped GaN buffer of 1.8 µm on a Si substrate of 1 mm thickness. They were isolated by Ar^{+}-implantation between two Ohmic contacts (see Figure 1). Isolation was achieved on all wafers in this study with an implantation dose of $7x10^{13}$ Ar^{+}-ions/cm^{-2} and an energy of 230 keV. While the details of the buffer and nucleation layers varied

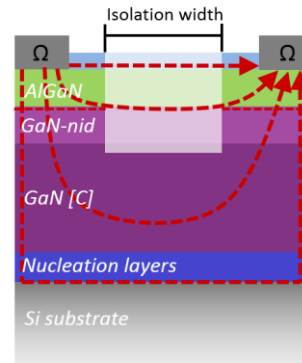

Fig. 1: Schematic representation of the AlGaN/GaN structures investigated in this work showing possible leakage current paths as well as the isolation width.

between the wafer lots investigated, the same isolation technique and parameters were used on all wafers. Seven wafers of four different wafer lots were measured. While lot A and B were fabricated with one epitaxy recipe, lot C and D have been produced under different conditions. In this way two different epitaxy recipes have been included in this work to study the effect of epitaxial details on isolation leakage currents. Different test structures were available with varying isolation width (and consequent contact separation) from 3 to 30 µm. While an increasing contact separation is used for the assessment of the dependence of leakage current on lateral electric field strength, taking I-V characteristics with different substrate biases ranging from 0V to 100V in 10V steps enables the assessment of the effect of the vertical electric field strength. In general, I-V characteristics have been performed with a floating substrate, unless otherwise stated. The influence of temperature on conduction laterally and vertically on the structure has been investigated by heating the chuck of the probe station from room temperature (between 25 and 29°C) to 50, 100, 150 and 200°C. Device operating temperatures are thus taken into account on the isolation leakage current.

RESULTS

Figure 2 shows I-V characteristics for two different isolation widths, 3 µm (triangles) and 15 µm (squares). While 15 µm is representative of the isolation width used for AlGaN/GaN power devices fabricated at CEA-Leti, test structures with an isolation width of only 3 µm aim at showing the effect of an increased lateral electric field. Figure 2 shows this effect with a general higher leakage current for isolation widths of 3 µm (represented as triangles). The figure further shows I-V characteristics of two different wafers of the same wafer lot. While current levels are identical below 100V, exponential behavior

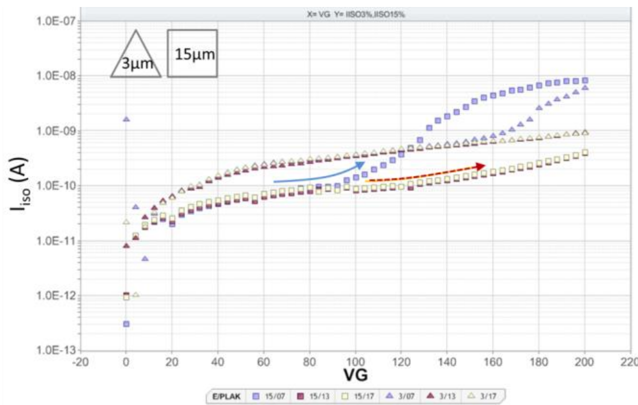

Fig. 2: IV characteristics of several wafers for an isolation width of 3µm (triangles) and 15µm (squares). The electronic signature of the buffer is visible in the onset of the exponential regime at different voltages for structures with morphological defects on Lot B Wafer 2 (blue) compared to reference structures without defects on Lot B Wafer 1(red and yellow superposed).

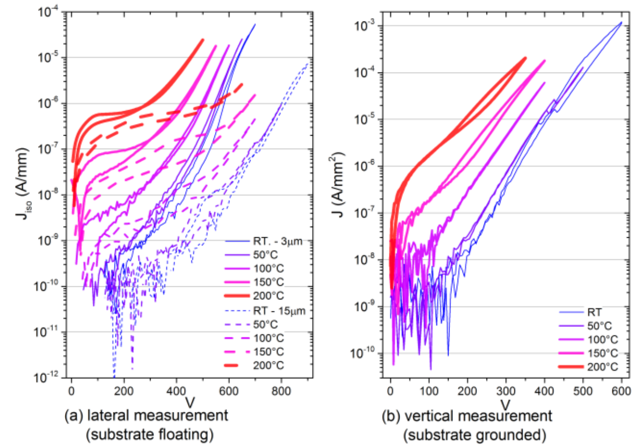

Fig. 3: Representative IV characteristics of test structures of Lot B Wafer 2 measured across isolation widths of (a) 3µm and 15µm with the substrate floating and (b) vertically across the structure with the substrate grounded.

occurs at lower voltages for wafer 2 in blue compared to wafer 1 in yellow. Observation of the two wafers reveals morphological defects on the surface of wafer 2, very likely linked to defects in the buffer layer. The figure therefore indicates an influence of defects onto the leakage current as well as being consistent with the hypothesis of buffer conduction linked to exponential behavior.

I-V characteristics, sweeping up to 800V, again for isolation widths of 3 and 15 µm, are shown in Figure 3 for (a) a lateral measurement between two Ohmic contacts with floating substrate as illustrated in Figure 1 and (b) a vertical measurement between one of the Ohmic contacts and the substrate grounded. Three distinct conduction regimes were identified in the lateral I-V characteristics of the device: An Ohmic regime below 100V, an intermediate exponential regime up to around 400V and a final performance limiting exponential regime above 400V. The Ohmic regime, dominant at low voltages, remained unchanged with variations in epitaxial material. Activation energies extracted in this regime for all wafers measured of this study (see Figure 4) are independent of the epitaxial

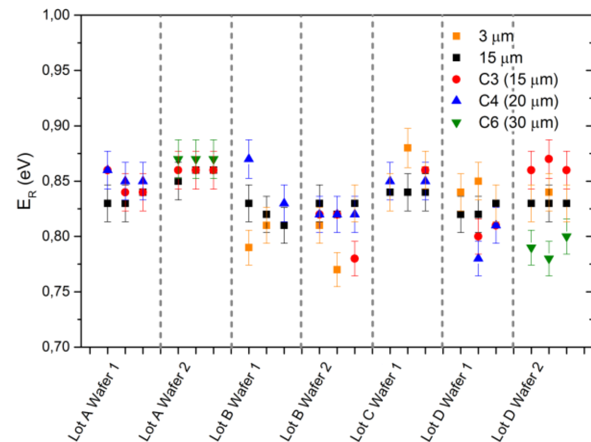

Fig.4: Activation energies extracted from the Ohmic regime of several wafers and isolation structures.

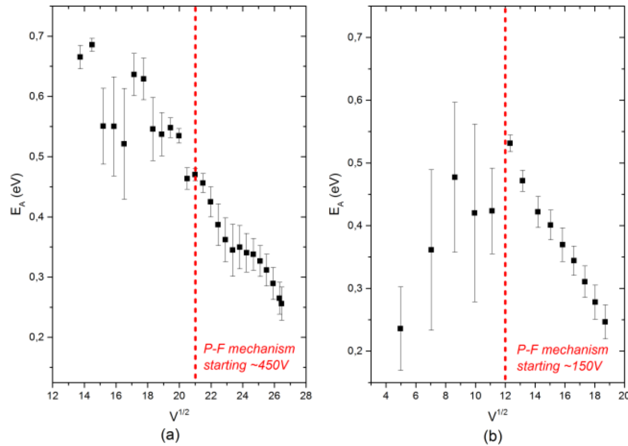

Figure 5: Activation energies extracted from an Arrhenius plot for (a) a lateral measurement configuration between the two contacts depicted in Figure 1 and (b) a vertical measurement configuration, i.e. measuring current between a biased contact on top of the AlGaN barrier and a grounded substrate.

structure. Figure 4 shows an average activation energy for the Ohmic conduction regime of around 0.85eV for all wafer lots. Equally, the current measured was unchanged below 100V (see Figure 2) suggesting that the conduction occurs across the implantation.

However, exponential regimes started dominating at voltages that varied with epitaxial layers (Figure 2) as well as with electric field strength (Figure 3). It is therefore proposed that these regimes are associated with paths across the buffer or the buried interfaces (such as the nucleation layer/substrate interface), consequently including a vertical contribution across the structure. This picture is further confirmed by vertical measurements across the device layers (substrate grounded) showing only the exponential behavior (Figure 3 (b)). The activation energies extracted for one representative example of lateral and vertical measurements are shown in Figure 5 depicting the onset of a straight line around 450V and 150V for lateral and vertical measurement, respectively. This linear relationship is consistent with the Poole-Frenkel mechanism and further indicates the presence of a vertical contribution to leakage current across device isolation at high voltage, confirming previous results in literature [11]. A barrier height of 1.5-1.9 eV could be extracted for wafers lots A and B from this linear relationship. However, it is not clear what this barrier physically corresponds to in the structure under investigation here.

As previously shown in Figure 2, decreasing the width of the implantation region increases the lateral electric field strength between Ohmic contacts resulting as expected in an increase in leakage current for all voltages. Further, the decreased width also results in an earlier onset of buffer conduction as can be seen in the exponential regime dominating earlier for an isolation width of 3 µm (Figure 3 (a)). In turn, positively biasing the substrate which reduces the vertical electric field moved this onset of exponential behavior to higher voltages. In Figure 6 it

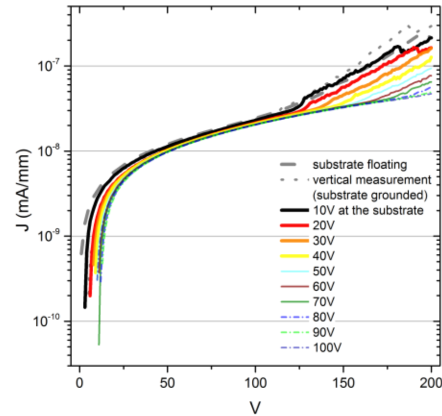

Fig.6: I-V characteristics with increasing substrate bias of Lot A Wafer1.

can be seen that gradually increasing the substrate bias for lateral voltage sweeps results in a later on set of the exponential current dominating over the Ohmic current. The activation of this second conduction path is therefore pushed to a higher bias. A substrate bias of at least 80V even succeeds in maintaining an Ohmic current throughout the 200V sweep. This further confirms the association between the exponential regime and an activation of conduction via the buffer.

Time-dependent measurements at room temperature were performed to further investigate the nature of conduction in the Ohmic regime in order to confirm the hypothesis of conduction across isolation at these voltages. Three measurement configurations were used on a test structure with a small and a roughly 20x larger contact to produce the results in Figure 7. As illustrated at the top of Figure 7, current is measured at the Ohmic contacts on top of the AlGaN barrier under different conditions. In black current is measured with a bias of 50V applied at the smaller contact (the larger contact grounded) and the substrate floating. In red the current is measured with the bias applied at the larger contact (substrate floating, small contact grounded) while in orange the current is measured with 50V applied at the smaller contact, the other grounded and the substrate biased at 50V. In all cases solid lines show the current measured at the smaller contact and dotted lines show current measured at the larger contact. A comparison between black and red curves shows that a capacitive effect with time constants up to 2 minutes is linked to a vertical conduction. This can be seen with the increased current level for a bias applied at the larger contact. Secondly, the exponential decrease is almost absent for current measured at ground which will have followed a path across the implantation area directly, possibly via a hopping mechanism, as the bias was kept at 50V, therefore in the Ohmic regime. The third configuration, shown in orange, creates zero electric field underneath the biased top contact, so that all current measured here should pass across the implanted area towards ground. The current level should therefore roughly

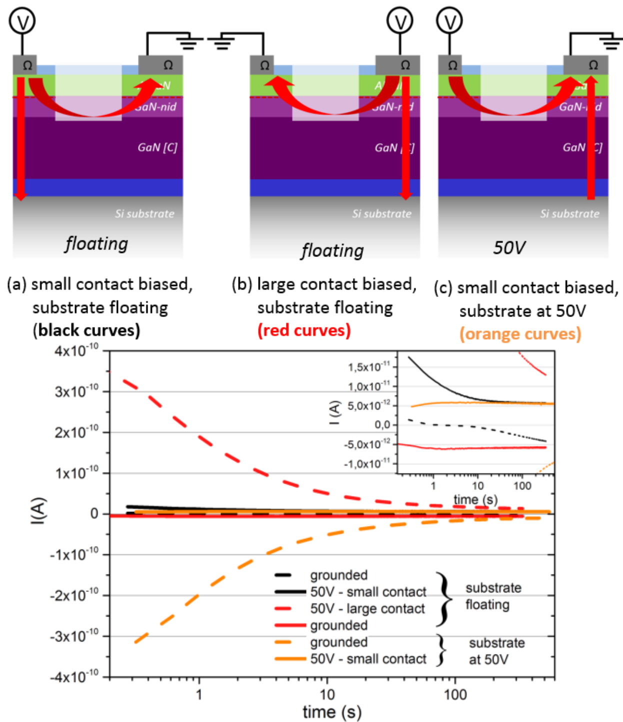

Fig. 7: I(t) across isolation between two Ohmic contacts at 50V with the substrate floating (black and red) showing the effect of vertical leakage through current depending on contact area (black solid compared to red dashed) as well as with 50V at the substrate (orange) confirming the association of the long time constants with a vertical current contribution (orange dashed).

correspond to that measured at ground for the other two measurement configurations. Indeed, the inset in figure 7 shows that the absolute value of the current measured in red and orange at the small contact (solid lines) is the same. The effectiveness of ion implantation to interrupt the 2DEG can also be seen from these results by noting the leakage current to be in the order of only fA. The fact that the larger contact was grounded in the black configuration results in a masked isolation current level as vertical fields due to self-induced polarization by the floating substrate may create a vertical current. Vertical capacitive conduction is further confirmed with equal current level at the large contact in orange and red (dashed curves).

Time constants of up to two minutes found in these measurements of I(t) therefore result in a general overestimation of the current in I-V sweeps below 100°C due to vertical leakage in the structure. Figure 7 shows that after an exponential decrease with time, the current converges to a constant level which estimates resistances of several TΩ with conduction between Ohmic contacts at 50V. Together with the time constants extracted, weak capacitances of 2-3 pF are found to be present in the measurement. The strong resistances associated with the current path make isolation IV characteristics therefore particularly susceptible to even small capacitances.

CONCLUSIONS

Ohmic and exponential regimes, as identified in I-V characteristics, represent the activation of different conduction paths across the isolation test structure. Through additional measurements it was shown that the Ohmic regime is associated with conduction across the implanted area itself (possibly through a hopping mechanism) while the exponential regime is dependent on the epitaxial layer structure and lead to premature breakdown of the structure at high voltages. As structures with morphological defects showed an earlier onset of vertical conduction, i.e. of the exponential regime, these short measurements represent further an early process quality control tool to quickly assess the epitaxial uniformity across a set of wafers. An analysis of I(t) not only estimates resistances of several TΩ for the conduction in the Ohmic regime, but also the effect of a weak capacitance of 2-3 pF. A detailed analysis of this mechanism needs to be conducted in the future to not only shed light on leakage currents across both the device isolation and also in AlGaN/GaN power devices in the off-state.

ACKNOWLEDGEMENTS

This work was funded by the laboratory of excellence network, GaNeX.

REFERENCES

[1] O. Hilt et al., “Normally-off GaN Transistors for Power Applications”, J Phys: Conf Series **494**, 012001 (2014).

[2] J. Möreke et al., “Effect of gate shaping and consequent process changes on AlGaN/GaN HEMT reliability”, Phys. Stat. Sol. A **209**, p.2646-2652, (2012).

[3] M. Sun et al., “Comparative Breakdown Study of Mesa- and Ion-Implantation-Isolated AlGaN/GaN High-electron-mobility-transistors on Si substrate”, Appl. Phys. Exp., **5**, 074202 (2012).

[4] R. Escoffier et al., “GaN HEMTs on silicon for power devices”, IEEE Int. SOI Conf., p.1-2, (2012).

[5] M.J. Uren and M. Kuball, “GaN Transistor Reliability and Instabilities”, 10th Int. Conf. on Adv. Semic. Dev. & Microsyst. (ASDAM), p.1-8, (2014).

[6] G. Meneghesso et al., “Breakdown mechanisms in AlGaN/GaN HEMTs: An overview”, Jap. J. of Appl. Phys. **53**, 100211 (2014).

[7] P. Moens et al., “Impact of buffer leakage on intrinsic reliability of 650V AlGaN/GaN HEMTs”, IEDM Tech. Dig., p.903-906, (2015).

[8] C. Zhou et al., “Vertical Leakage/Breakdown Mechanisms in AlGaN/GaN-on-Si Devices”, IEEE Electr. Dev. Lett. **33**(8), p.1132-1134, (2012)

[9] M.J. Uren et al., “Electric Field Reduction in C-Doped AlGaN/GaN on Si High Electron Mobility Transistors”, IEEE Elecr. Dev. Lett. **36**(8), p.826-828, (2015).

[10] F.A. Marino et al., “Analysis of off-state leakage mechanisms in GaN-based MIS-HEMTs: Experimental data and numerical simulation”, Solid-State Electronics **113**, p.9-14, (2015).

[11] P. Srivastava et al., “Silicon Substrate Engineered High-Voltage High-Temperature GaN-DHFETs”, IEEE Trans. On Electr. Dev., **60** (7), 2217-2224 (2013)

[12] M.J. Uren et al., “Buffer transport mechanisms in intentionally carbon doped GaN heterojunction field effect transistors”, Appl. Phys. Lett. **104**, 263505, (2014).