GaN electronic devices

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Outline of the electronic module

Lecture I: Electronic devices

- Introduction
- Heterostructures
- Lateral devices: HEMTs

Lecture II: RF devices

- Equivalent circuit and FOM: important aspects
- Technologies to improve RF performance

Lecture III: Lateral Power devices

- E- and D-mode devices
- Reaching low resistance and high voltage
- current commercial technology
- Losses in GaN power devices

Lecture IV: Vertical Power devices

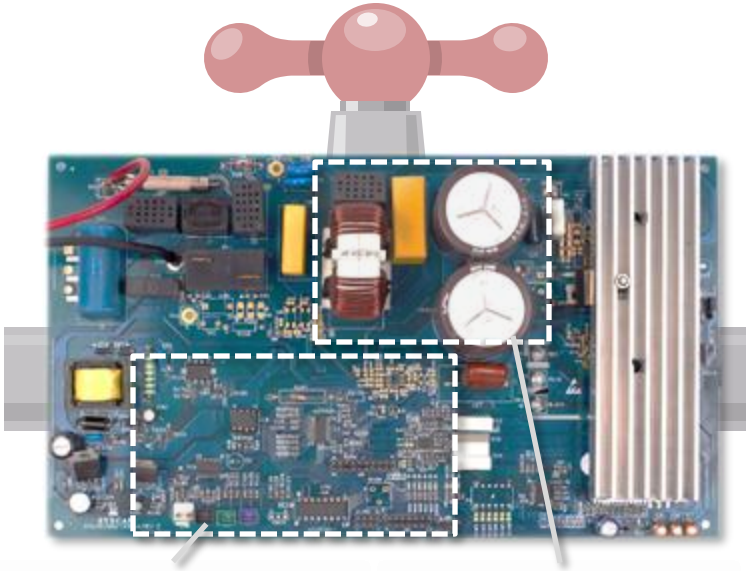
- Introduction
- Vertical devices: GaN PN diodes and MOSFETs
- Novel concepts in vertical power electronics

Bonus: Novel trends





Power Electronics

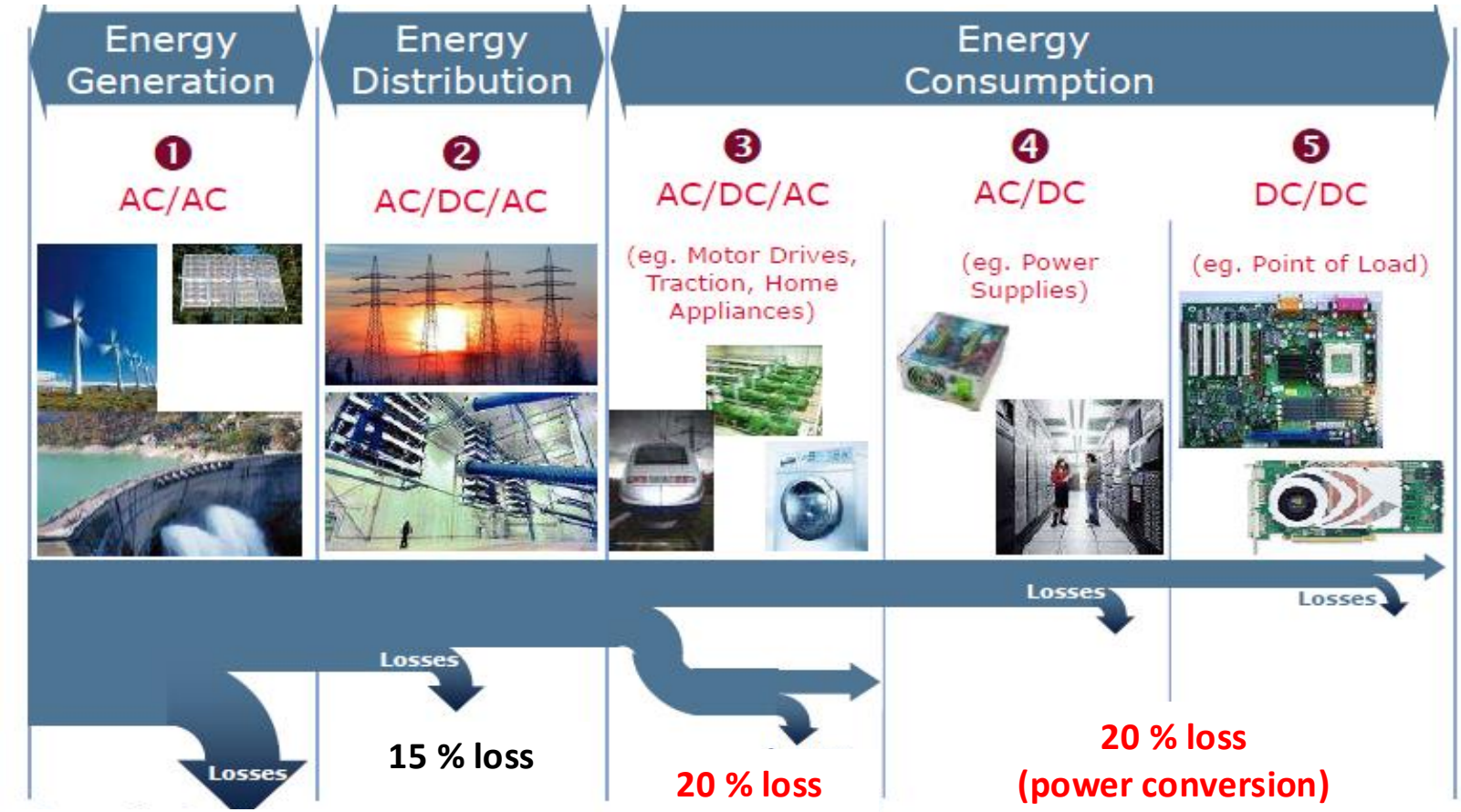


Semiconductor devices: transistors, diodes, and thyristors

Passive components: capacitors, inductors, transformers, etc.



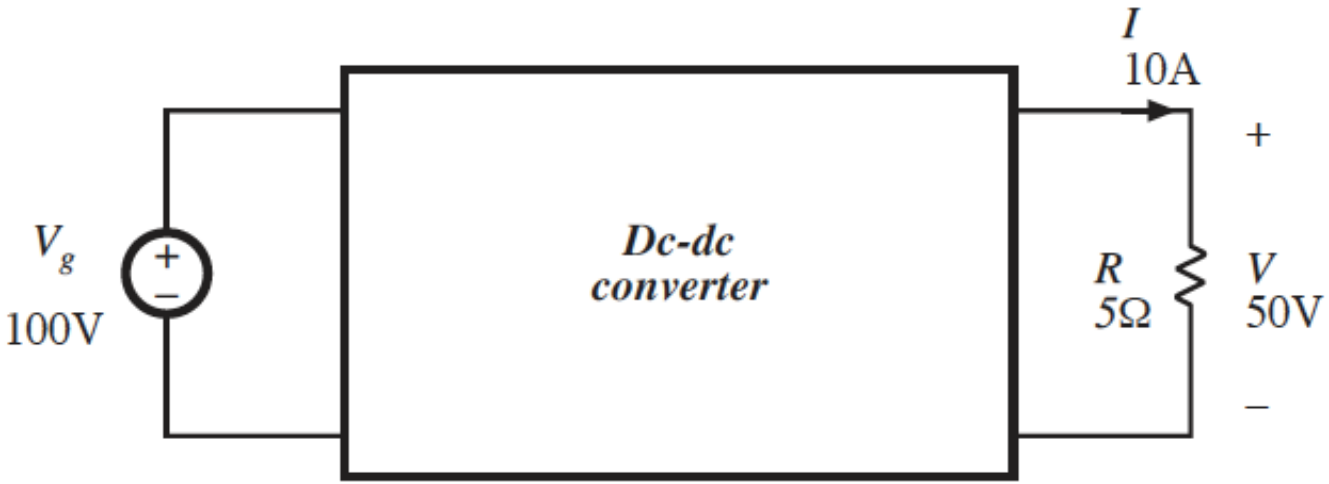
Motivation: Large losses in power conversion



Source: Infineon Technologies

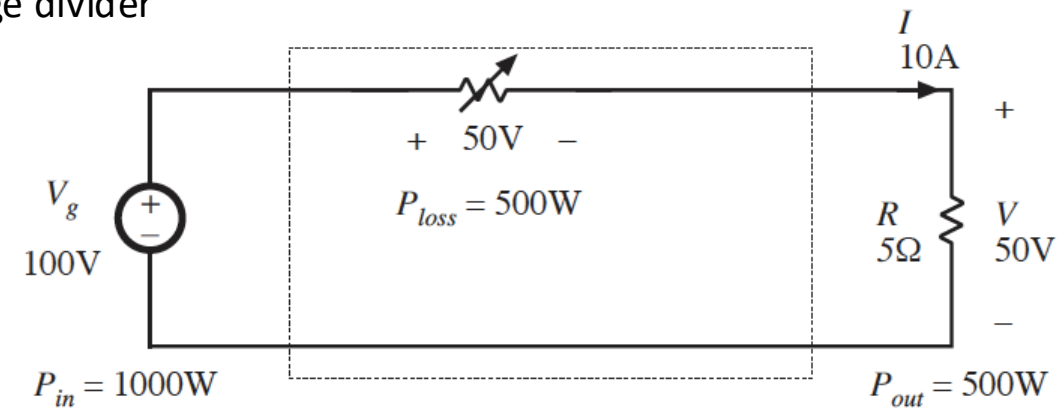
Poorer efficiency: higher thermal management requirements

DC-DC converter

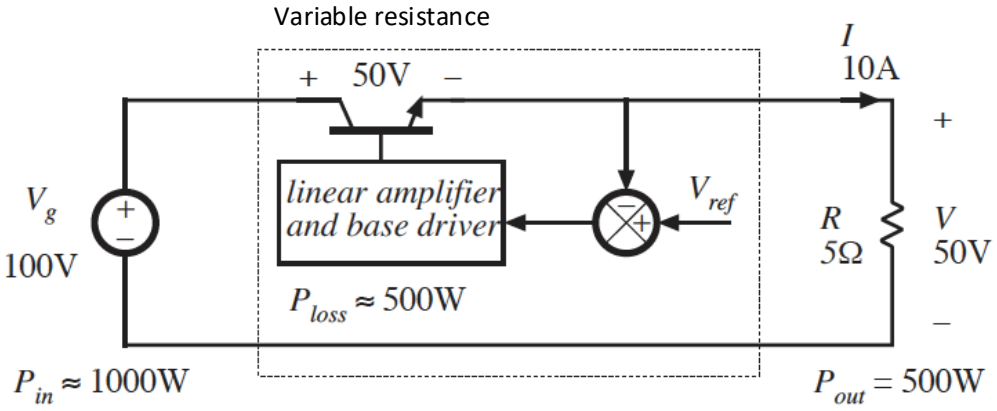


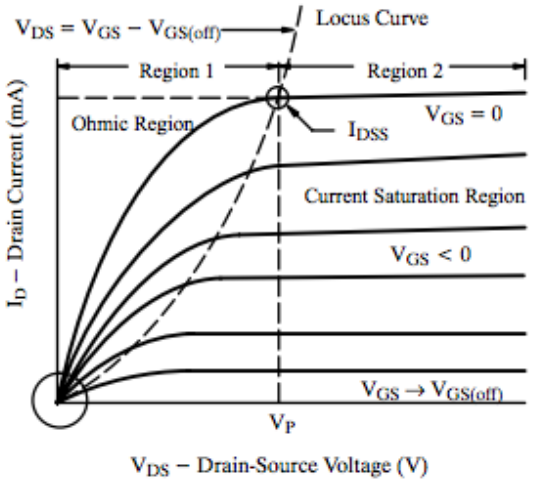
How can such converter be realised?

Solution 1: voltage divider



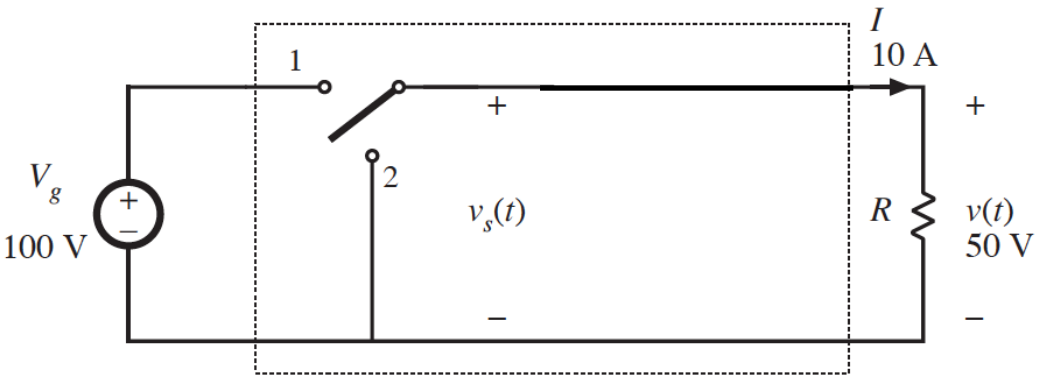
Solution 2: linear amplifier

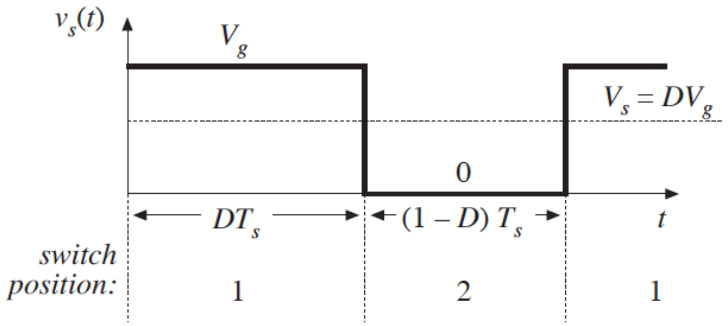




These are very inefficient solutions

Concept of switching





D = switch duty cycle

$0 \le D \le 1$

T_s = switching period

f_s = switching frequency

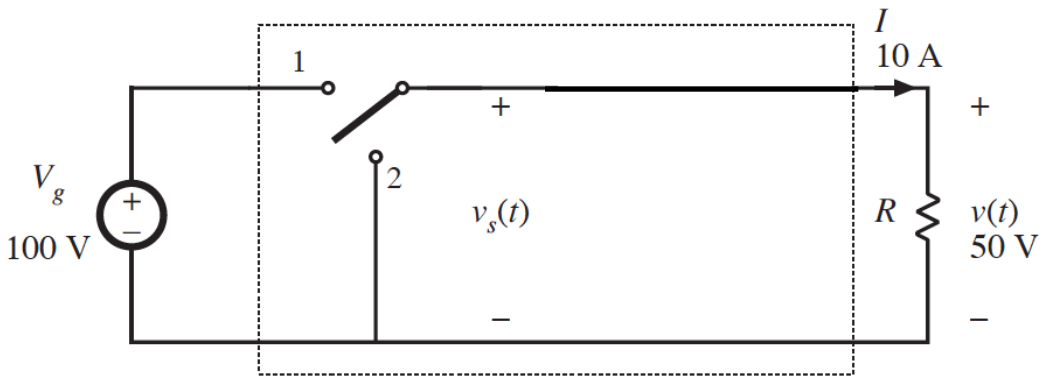
$= 1 / T_s$

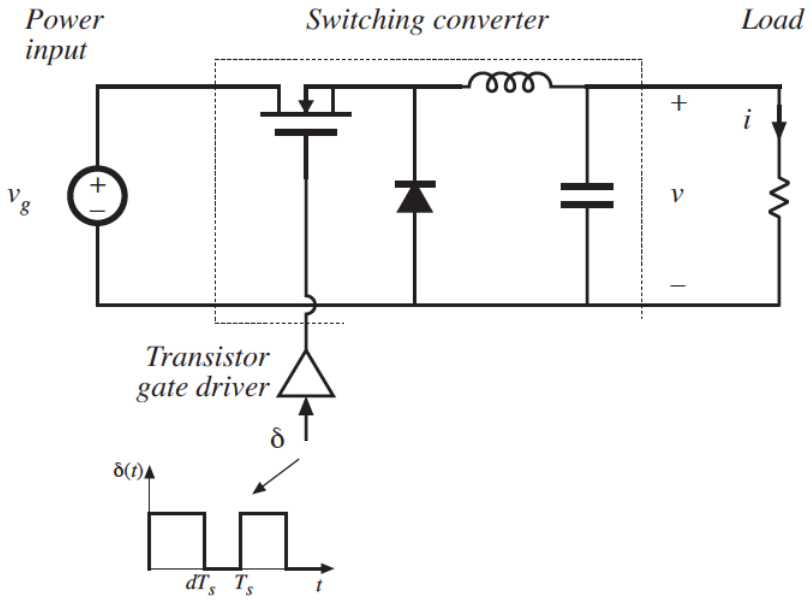
DC component of $v_s(t)$ = average value:

$$V_s = \frac{1}{T_s}\int_0^{T_s} v_s(t)\,dt = DV_g$$

Fundamentals of Power Electronics, Robert W. Erickson, Dragan Maksimović

Concept of switching





Device requirements

I. Static behavior

Reduce on-resistance (R_{ON})

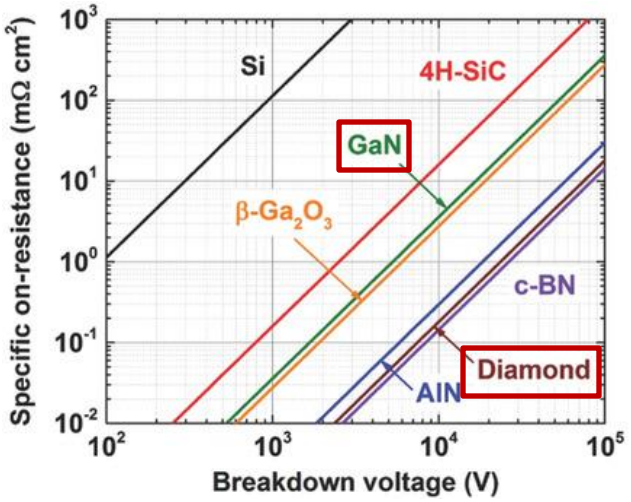
Increase breakdown voltage (V_{BR})

II. Dynamic behavior:

Low switching losses in power devices

Fundamentals of Power Electronics, Robert W. Erickson, Dragan Maksimović

Challenges of power switches



I. Static behavior

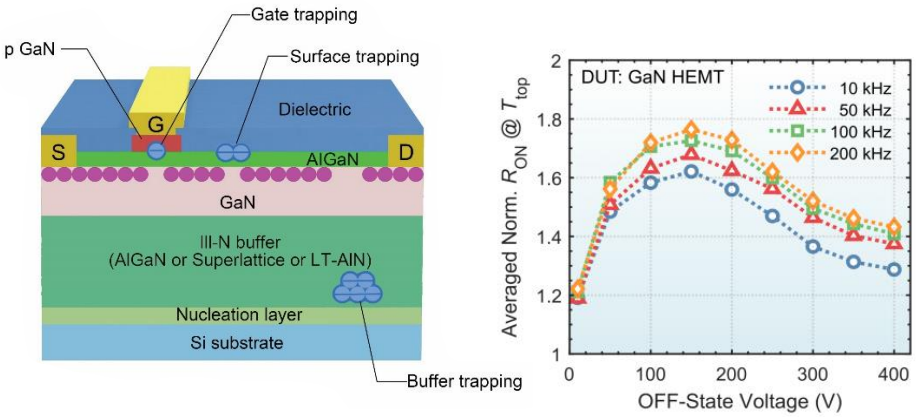
Reduce on-resistance (R_{ON})

Increase breakdown voltage (V_{BR})

Normally-off operation

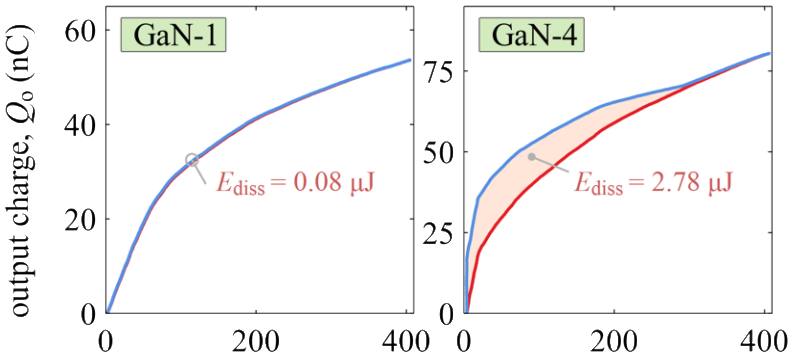
II. Dynamic behavior: switching losses in power devices

On-state: Dynamic $R_{DS,ON}$: Increase in R_{ON} during switching



H. Zhu and E. Matioli, **IEEE Transactions on Power Electronics**, 2023

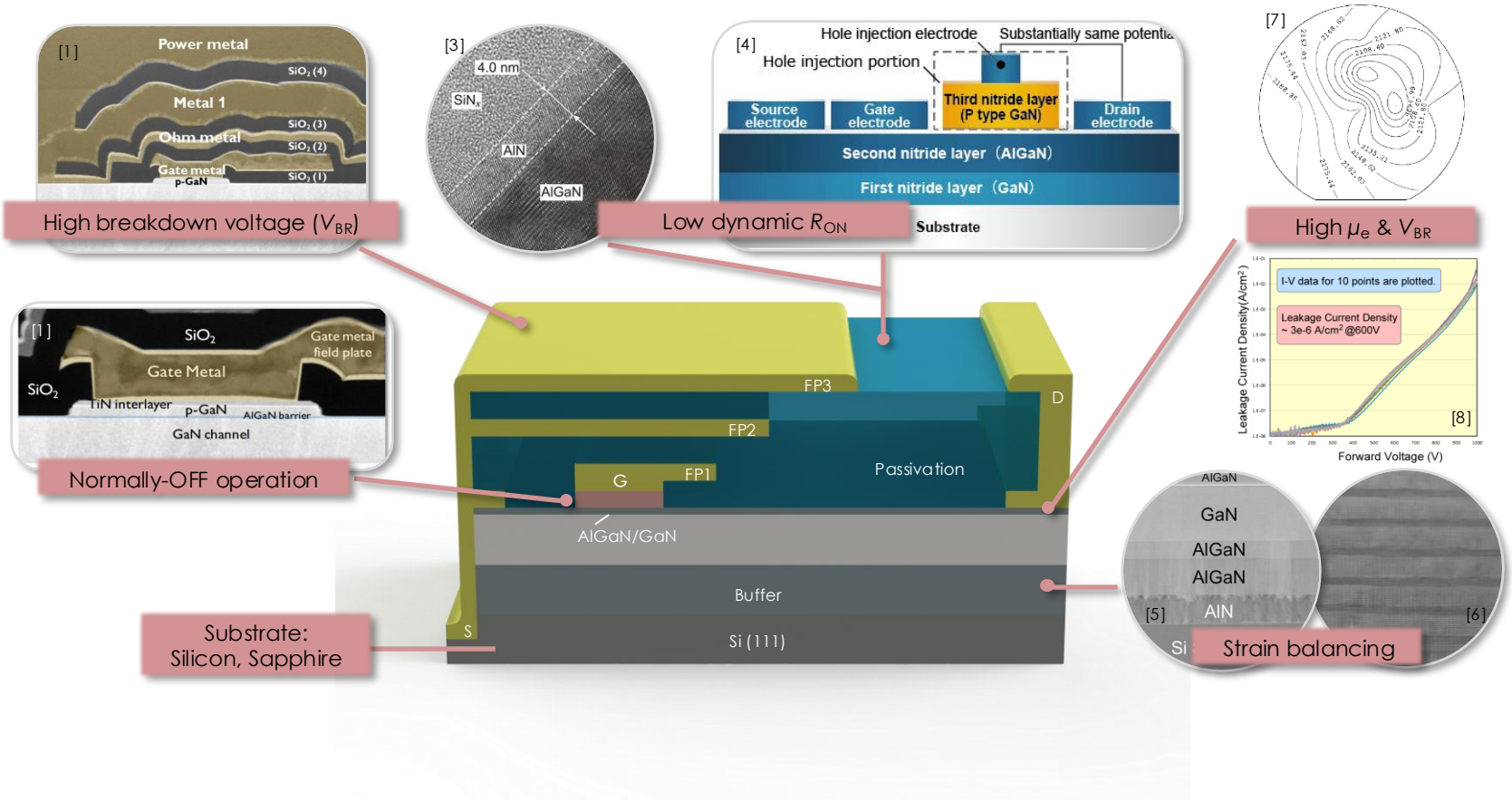
Off-state*: Unexpected losses from charging/discharg
output capacitance



N. Perera, A. Jafari, L. Nela, G. Kampitsis, M. S. Nikoo, and E. Matioli, IEEE COMPEL 2020

GaN power electronic device

Technologies involved in making a high performance power devices



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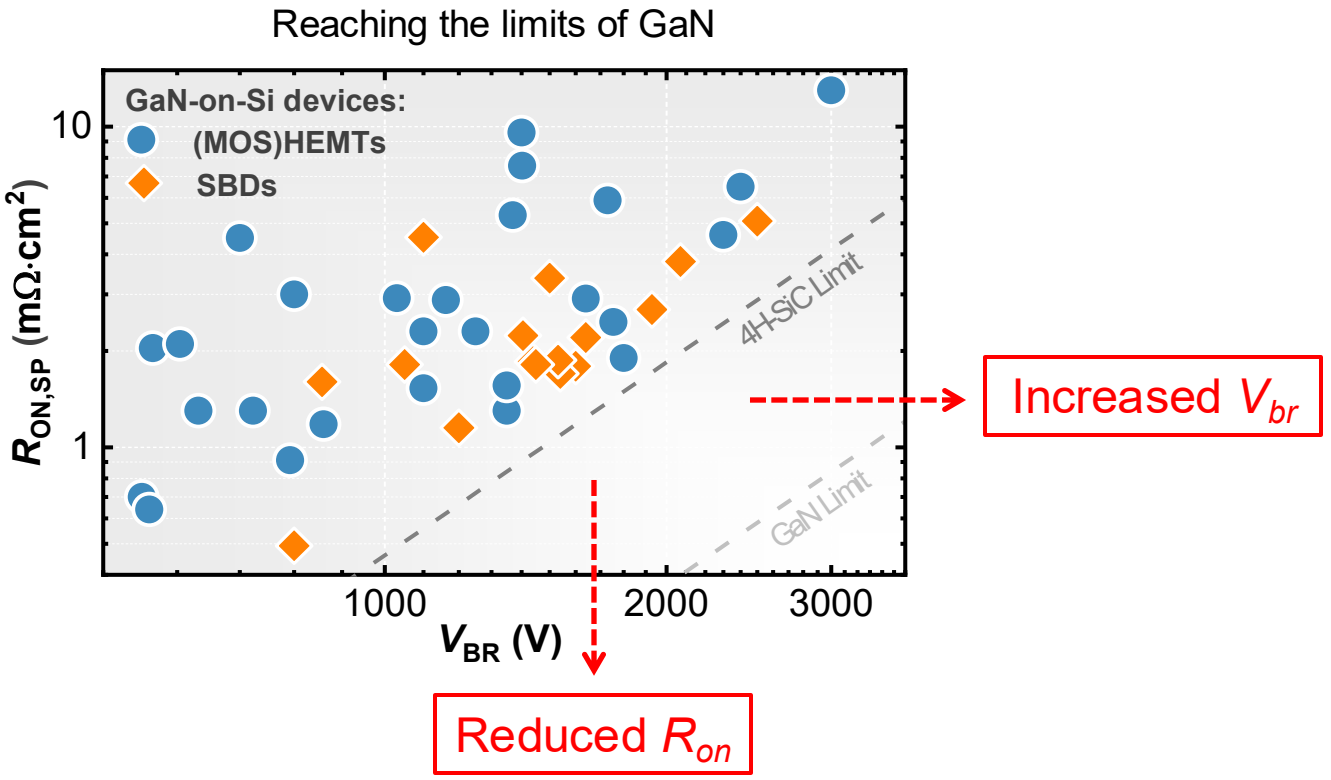
GaN for lateral power devices

Challenges of GaN-on-Si power devices

On a device level, the challenges are to reduce R_{ON} and increase V_{BR}



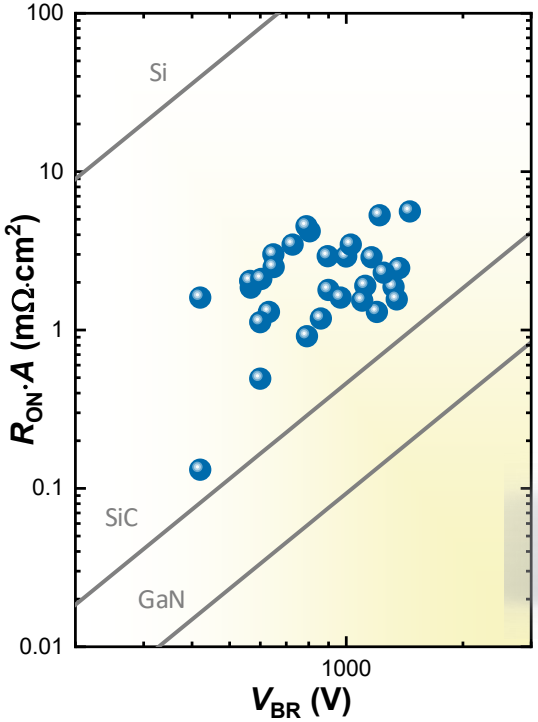
The goal for power electronics is to develop devices with:

- Normally-off operation with high V_{TH}
- High V_{BR}
- Ultra-low on-resistance

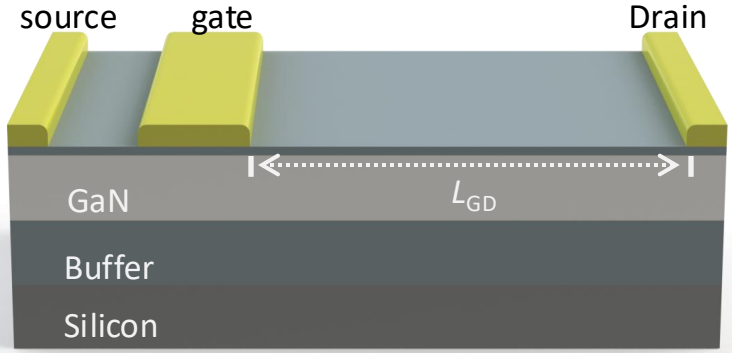
These are the static properties (but remember: switching is also important)

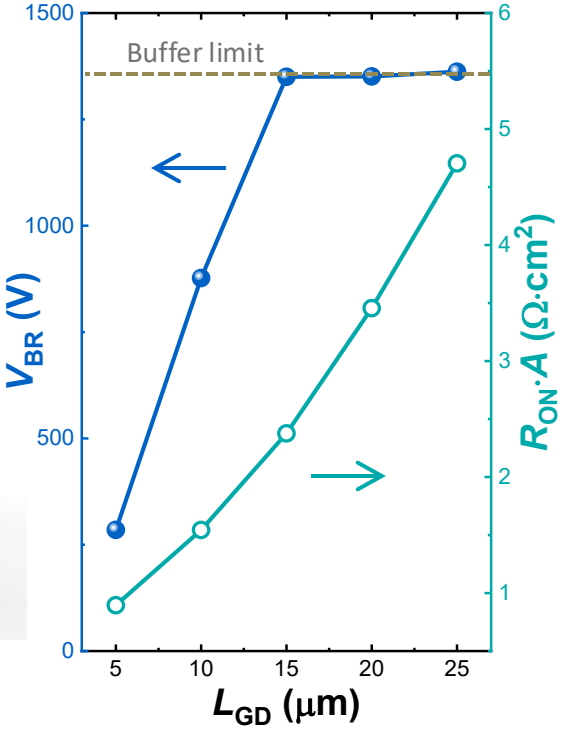
Trade-off between high breakdown voltage and low R_{ON}

Trade off between high V_{BR} and small R_{ON}



$$R_{ON} \cdot A \approx R_s \cdot \frac{L}{W} \cdot W \cdot L = R_s \cdot L^2$$

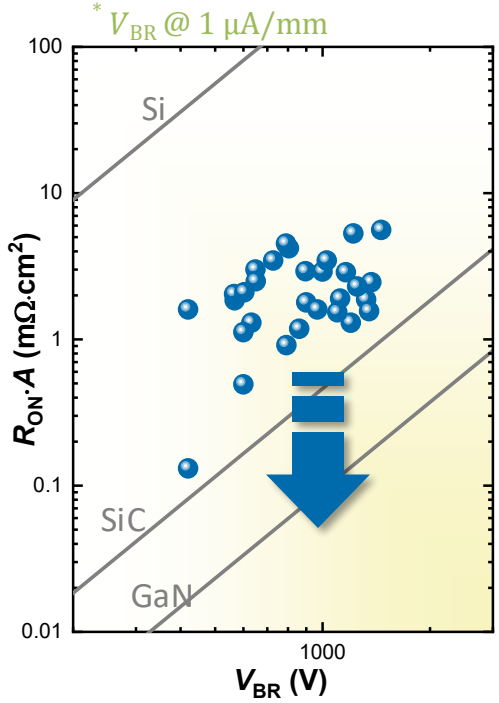




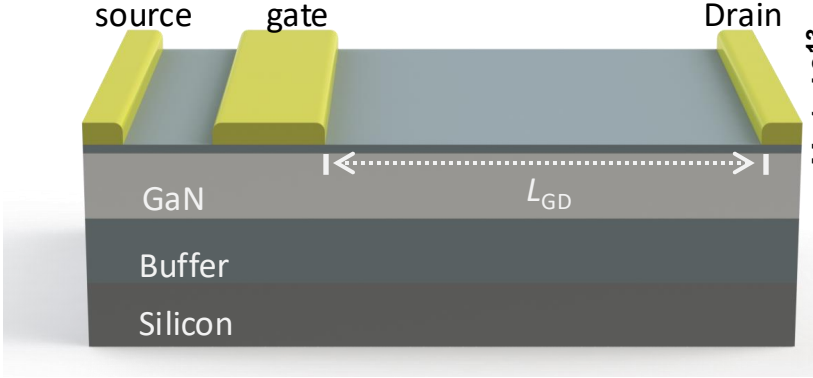
[1] IMEC, "Perspectives for disruptive 200 mm/8-inch GaN power device and GaN-IC technology," SEMICON Europa 2018. [2] http://uef.fei.stuba.sk/moodle/mod/book/view.php?id=7920&chapterid=87 [3] Y. Lu, Q. Jiang, Z. Tang, S. Yang, C. Liu and K. J. Chen, Appl. Phys. Express 8, 064101 (2015). [4] https://industrial.panasonic.com/kr/products/semiconductors/powerics/ganpower [5] https://compoundsemiconductor.net/article/99114-heat-sinking-gan-on-silicon-the-substrate-removal-challenge.html [7] http://en.enkris.com/cp/html/?31.html [6] https://www.researchgate.net/post/Determination_of_the_lattice_parameter_of_the_GaN_AlN_layers_of_a_superlattice_from_TEM_images [8] http://www.ntt-at.com/product/epitaxial/

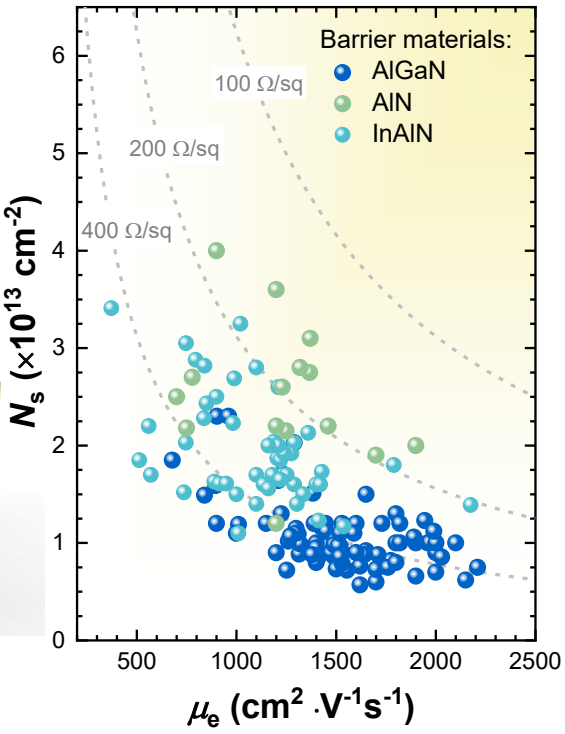
Trade-off between high breakdown voltage and low R_{ON}

GaN is a lateral devices: unlike in vertical devices **high V_{BR} requires larger device L_{GD}**



$$R_{ON} \cdot A \approx R_s \cdot \frac{L}{W} \cdot W \cdot L = R_s \cdot L^2$$





This sets a limit on R_{ON} and V_{BR}

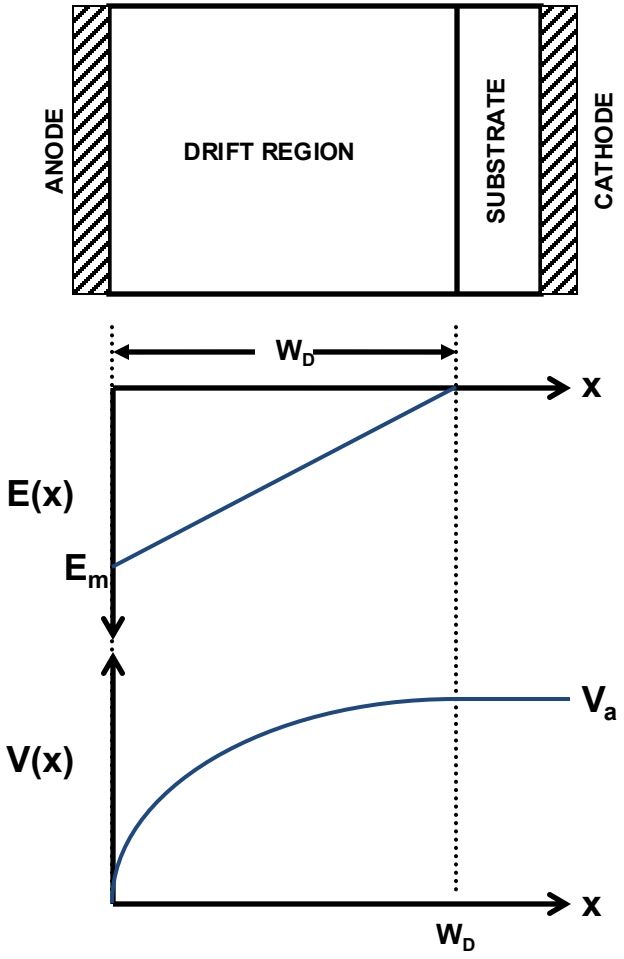
$$R_s = \frac{1}{q\mu n_s}$$

[1] IMEC, "Perspectives for disruptive 200 mm/8-inch GaN power device and GaN-IC technology," SEMICON Europa 2018. [2] http://uef.fei.stuba.sk/moodle/mod/book/view.php?id=7920&chapterid=87 [3] Y. Lu, Q. Jiang, Z. Tang, S. Yang, C. Liu and K. J. Chen, Appl. Phys. Express 8, 064101 (2015). [4] https://industrial.panasonic.com/kr/products/semiconductors/powerics/ganpower [5] https://compoundsemiconductor.net/article/99114-heat-sinking-gan-on-silicon-the-substrate-removal-challenge.html [7] http://en.enkris.com/cp/html/?31.html [6] https://www.researchgate.net/post/Determination_of_the_lattice_parameter_of_the_GaN_AlN_layers_of_a_superlattice_from_TEM_images [8] http://www.ntt-at.com/product/epitaxial/

Figures of merit

Vertical devices: drift region

Figure of merit for power devices: describing resistance versus breakdown voltage



$$R_{ON,SP} = \frac{W_D}{qN_D\mu_n}$$

$$V = \frac{E_m W_D}{2} \quad \text{thus} \quad W_D = \frac{2BV}{E_C}$$

Poisson's Equation:

$$\frac{d^2V}{dx^2} = -\frac{dE}{dx} = -\frac{Q(x)}{\varepsilon_S} = -\frac{qN_D}{\varepsilon_S}$$

$$E(x) = -\frac{qN_D}{\varepsilon_S}(W_D - x)$$

$E_c = qN_d/eps*W_D$

$$V(x) = \frac{qN_D}{\varepsilon_S}(W_D x - \frac{x^2}{2})$$

$E_c = 2V_{BR}/W_D = qN_dW_D/eps$

$V_{BR} = qN_dW_D^2/2eps$

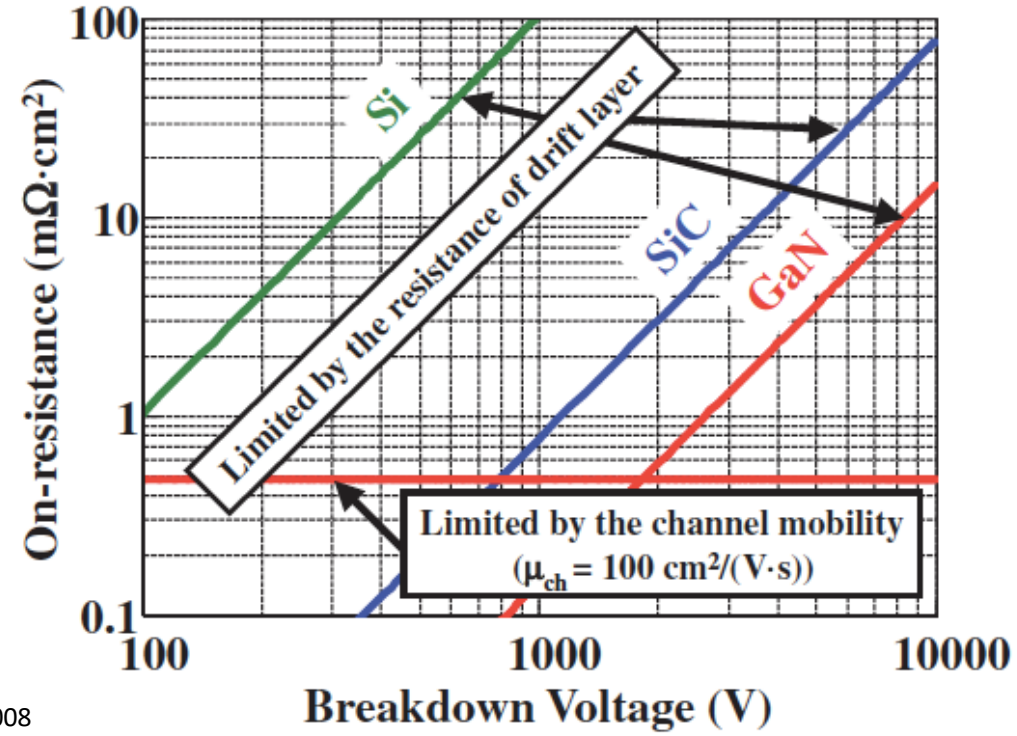
Vertical devices

Ideal Specific On-Resistance:

$$R_{ON,SP} = \frac{W_D}{q\mu_n N_D} \qquad N_D = \frac{\varepsilon_S E_C^2}{2qBV} \qquad W_D = \frac{2BV}{E_C}$$

$$R_{ON,SP} = \frac{4BV^2}{\varepsilon_S \mu_n E_C^3}$$

$$BFOM = \varepsilon_S \mu_n E_C^3 = \frac{4BV^2}{R_{ON,SP}}$$



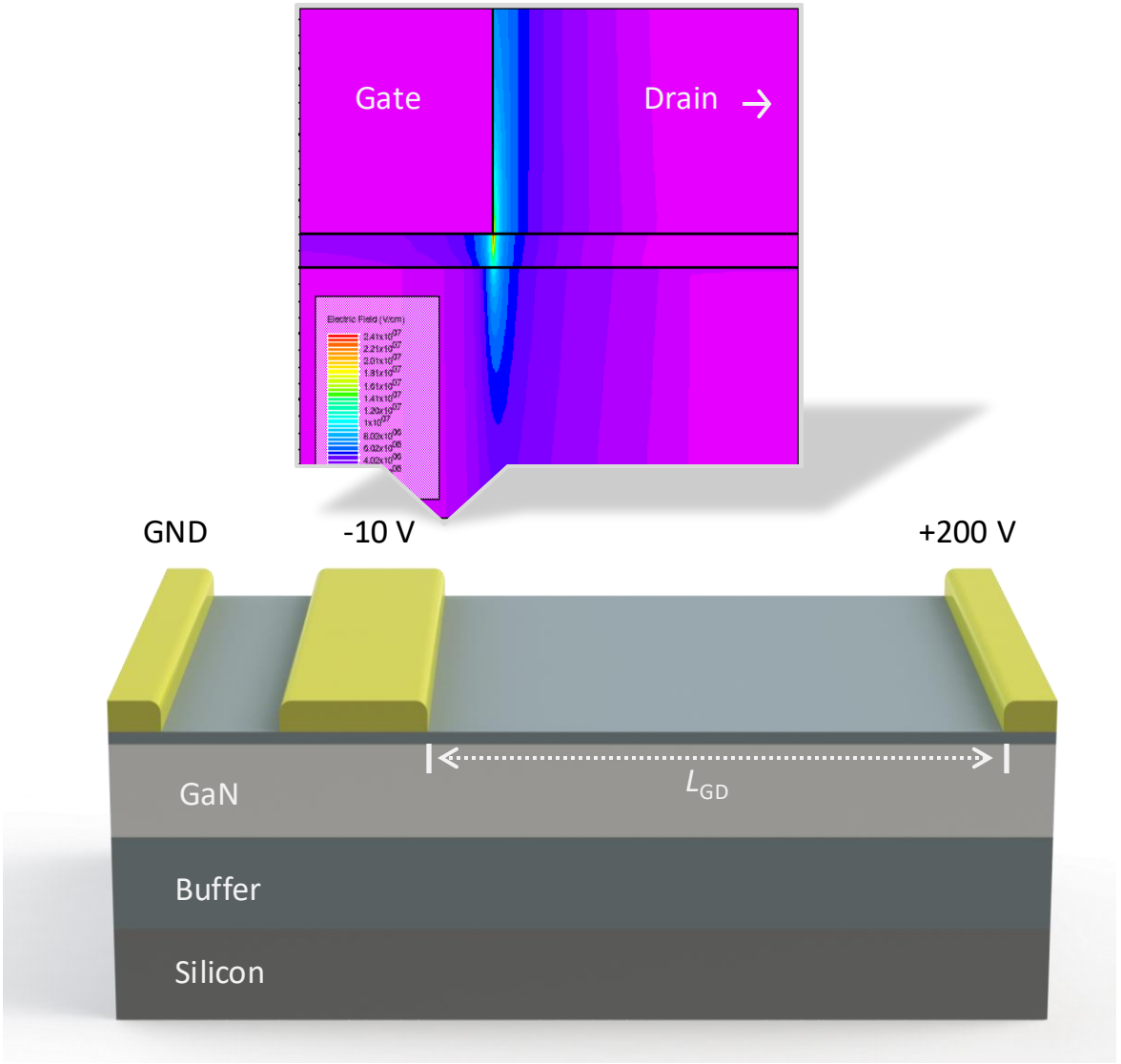
B.J. Baliga, *Fundamentals of Power Semiconductor Devices*, Springer 2008

	ε_r	μ_{bulk} [cm²/(V·s)]	E_c (MV/cm)
Si	11.8	1350	0.3
4H-SiC	10.0	720	2.0
GaN	9.0	900	3.3

Channel mobility limits the total resistance: MOS channel mobility is very important

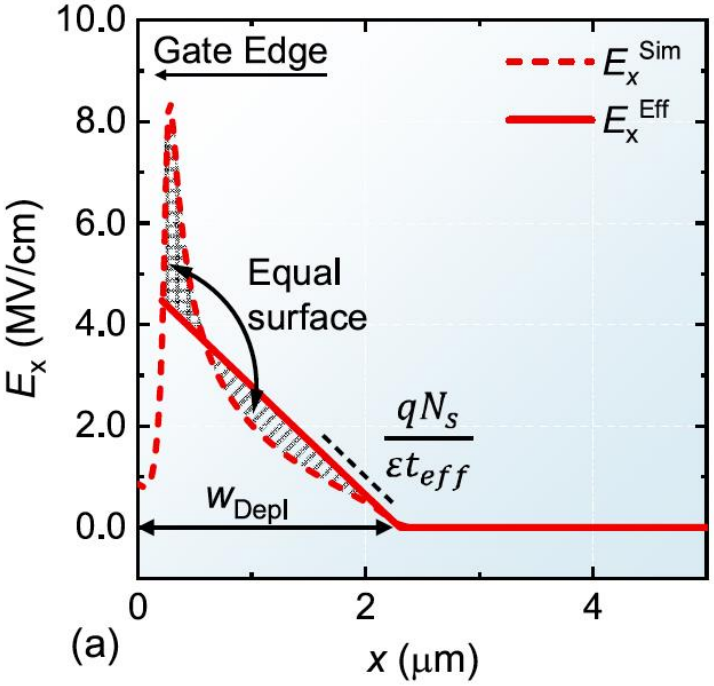
Can we use this FOM for lateral devices?

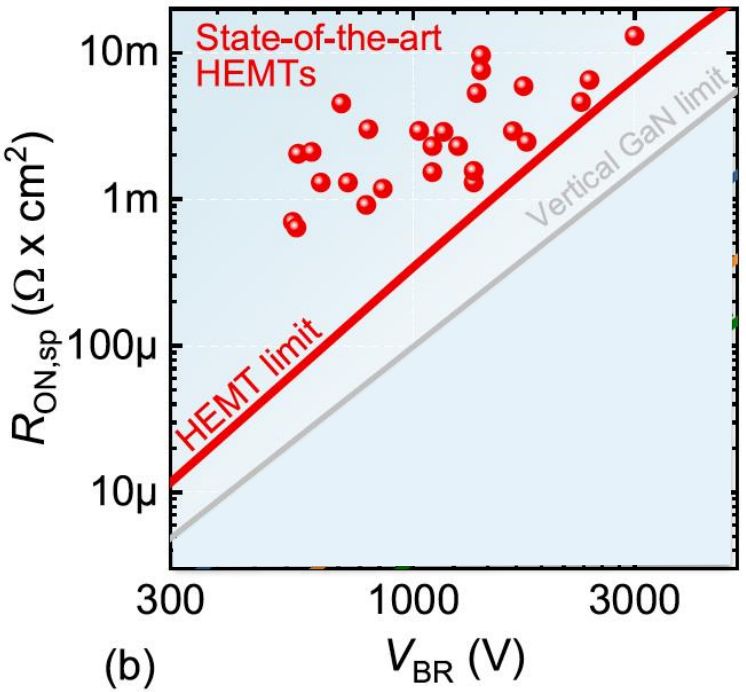
Figure of merit for lateral devices



Can we use this FOM for lateral devices?

Figure of merit for lateral devices





$$E_{x,\mathrm{HEMT}} = \frac{qN_{s,\mathrm{HEMT}}}{\varepsilon t_{\mathrm{eff}}}\left(x - W_{\mathrm{Depl}}\right)$$

Ideal Specific On-Resistance:

$$R_{\mathrm{ON,SP}} = \frac{L_D^2}{q\mu N_s}$$

$$V_{\mathrm{BR,HEMT}}[\mathrm{V}] = 2.5 \times 10^{15} \mathrm{x} \left(N_{s,\mathrm{HEMT}}\left[\mathrm{cm}^{-2}\right] / t_{\mathrm{eff}}[\mathrm{cm}]\right)^{-3/4}$$

$$R_{\mathrm{ON,sp,HEMT}}\left[\Omega \times \mathrm{cm}^2\right] = \frac{7 \times 10^{-9}}{\mu\left[\frac{\mathrm{cm}^2}{\mathrm{Vs}}\right]} V_{\mathrm{BR}}^{8/3}[\mathrm{V}]$$

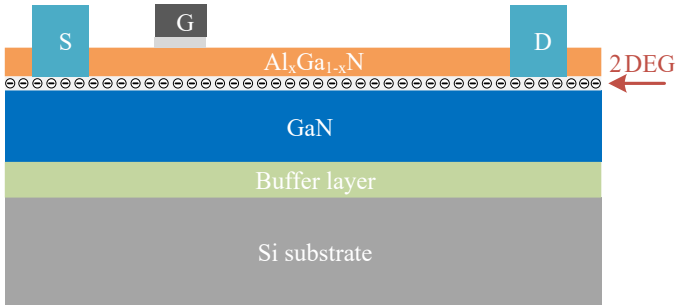
L. Nela, C. Erine, M. V. Oropallo and E. Matioli, ***IEEE Journal of the Electron Devices Society***, vol. 9, pp. 1066-1075, 2021

Enhancement mode (normally-off operation)

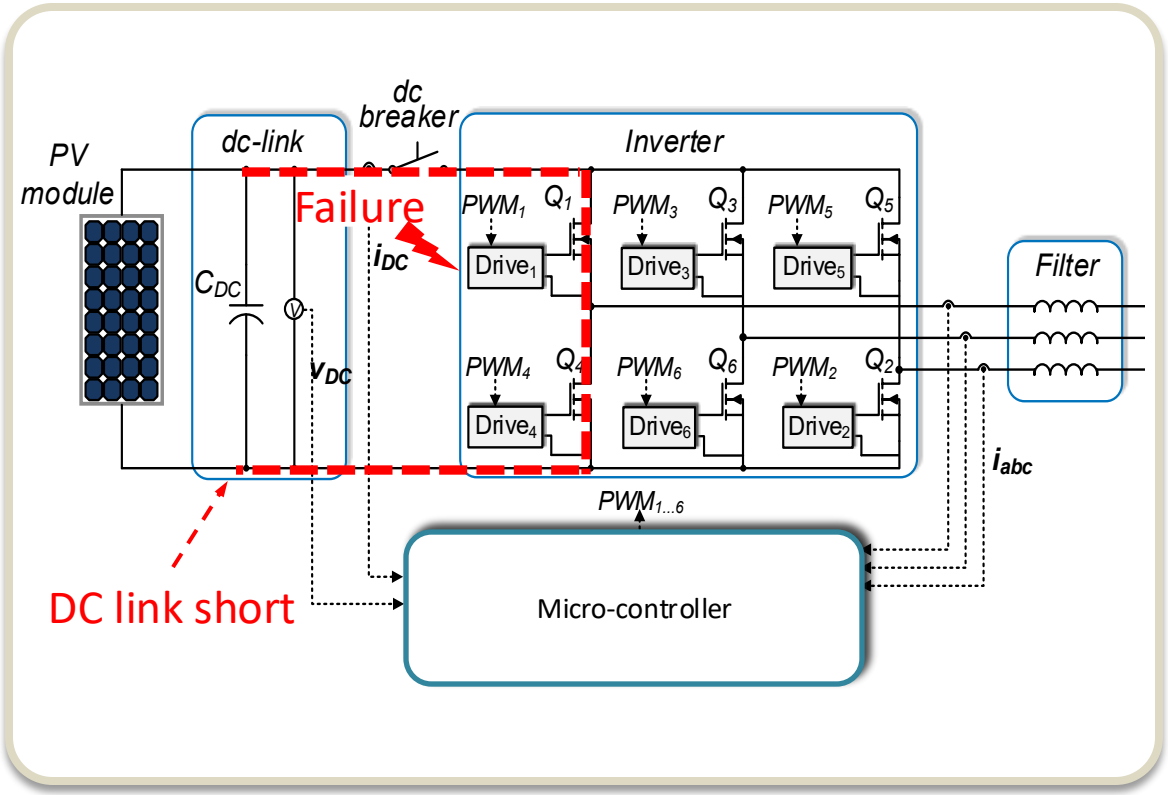
Enhancement mode (normally-off operation)

Why do we need enhancement mode?

HEMTs are naturally normally-on devices



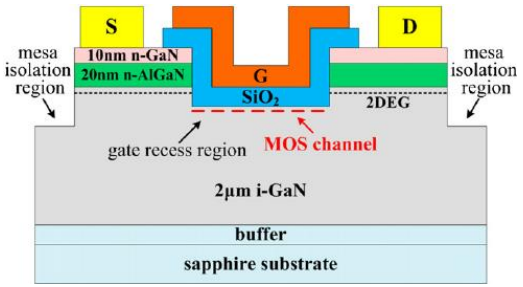
Fail safe operation



Normally-off operation is required!

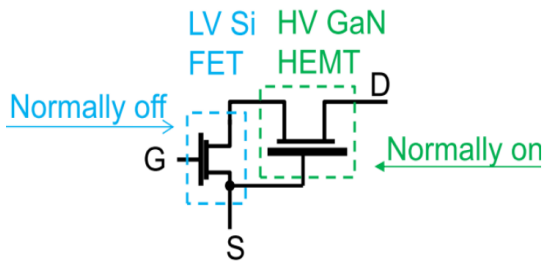
Enhancement mode (normally-off operation)

AlGaN barrier recess[2]



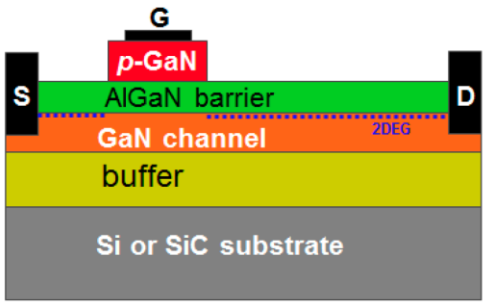
STMicroelectronics, CEA-Leti

Cascode configuration

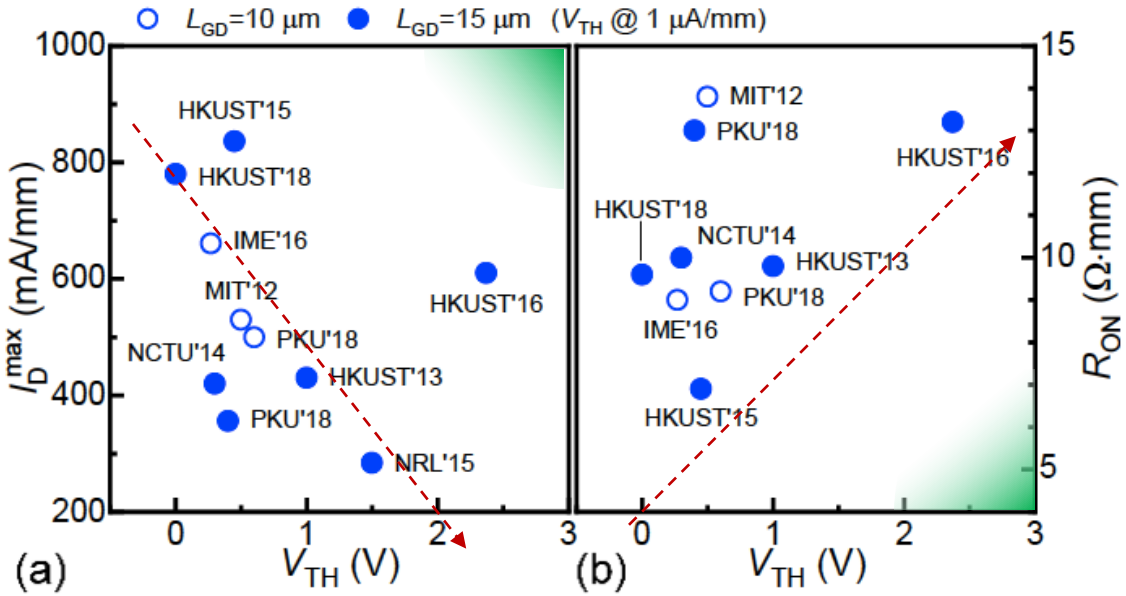


From transphorm/Nexperia

p-GaN cap layer[3]



Panasonic/Infineon/GaN systems/EPC

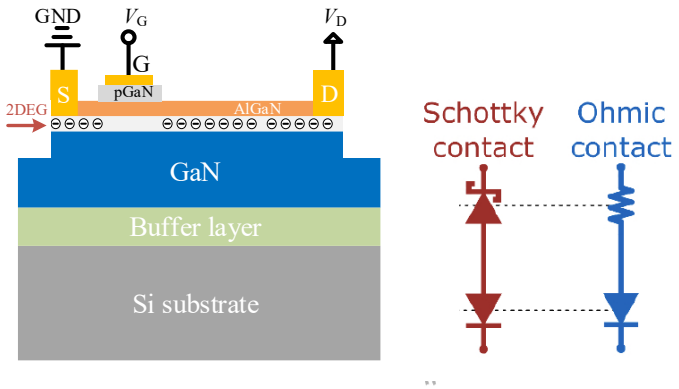


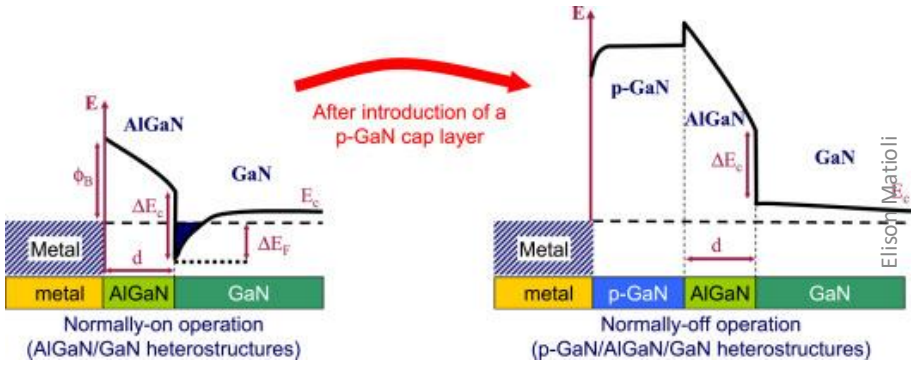
Trade-off between V_{th} and R_{ON}

Enhancement mode (normally-off operation)

P-GaN gates is the most commonly available solution: Gate can be ohmic or Schottky

pGaN gate E-mode





Advantages:

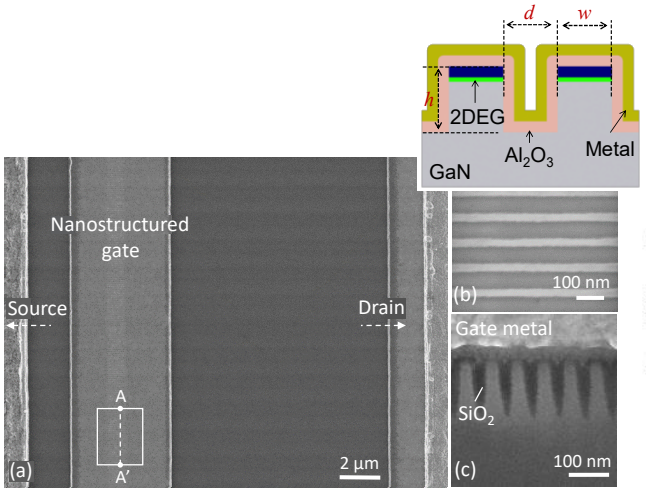
- Single transistor delivers E-mode
- Compatibility with current gate drivers (0-6V gate drivers)

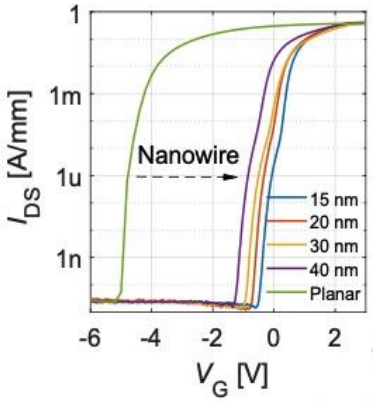
Challenges:

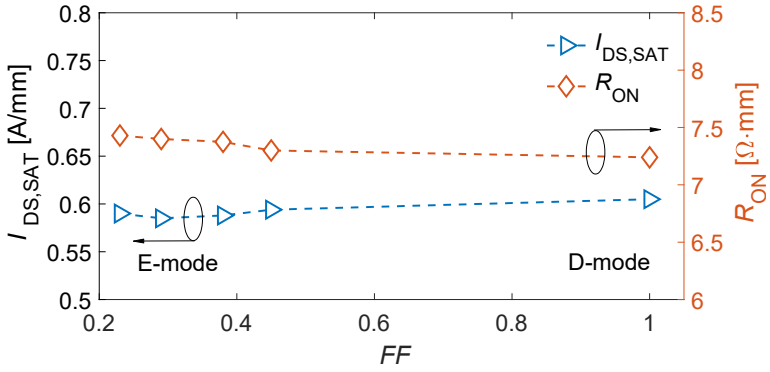
- Trade-off between Ron and Vth
- Introduces a gate diode: gate voltage swing is limited (~6–7 V).
- A higher positive gate bias can forward-bias or cause charge injection in the p-GaN gate structure. High leakage current.
- Gate reliability is thus a concern – even slight over-voltage can lead to permanent device degradation

Tri-gate for normally-off power transistors

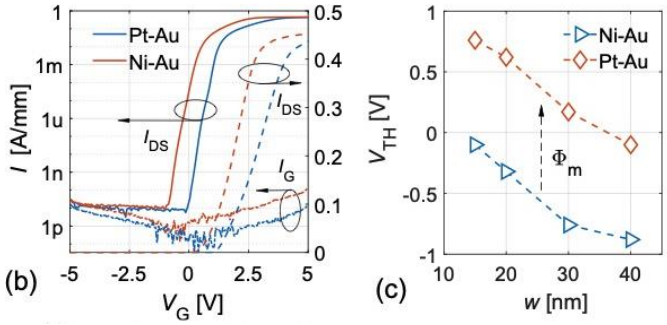
Nanowires + large work-function gate metal

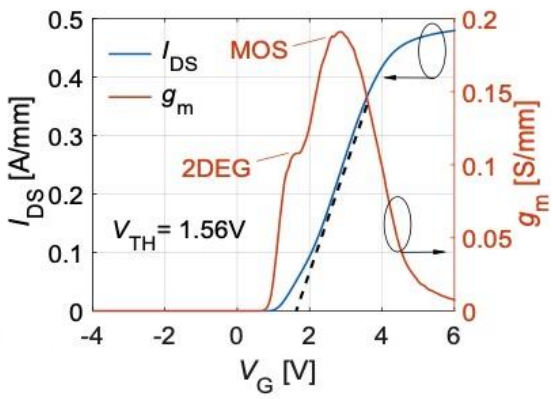


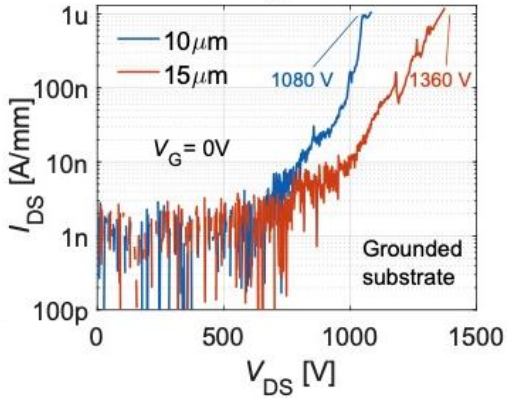




Large work-function metal : Pt instead of Ni







Nanowires for high voltage operation

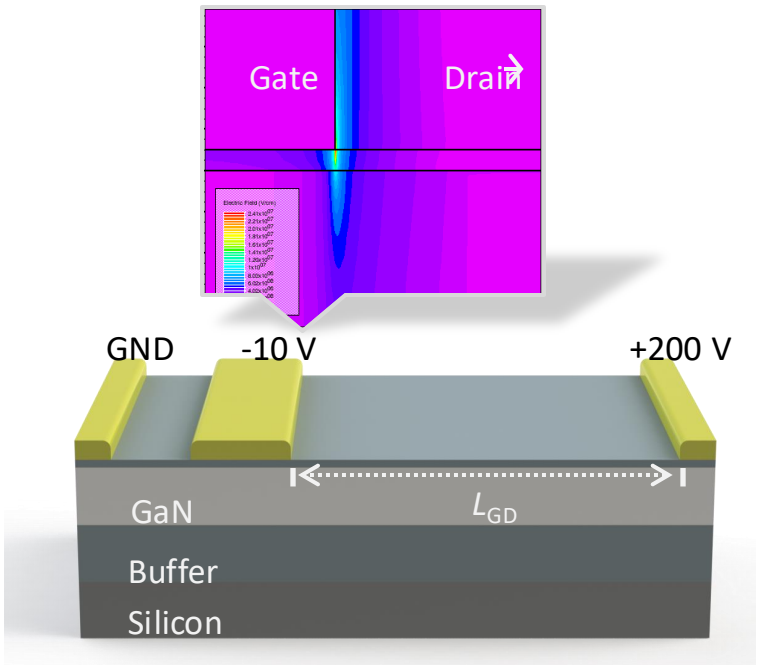
L. Nela, M. Zhu, J. Ma and E. Matioli, ***IEEE EDL***, vol. 40, no. 3, pp. 439-442, March 2019

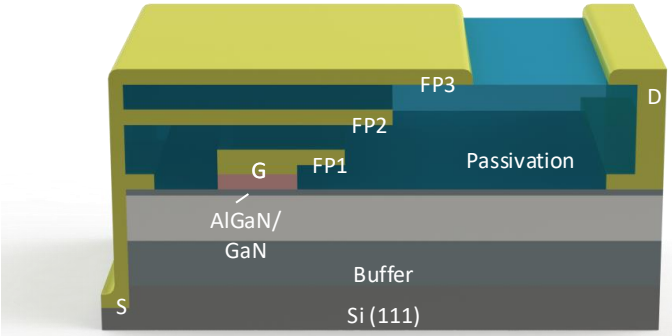
Higher voltage: managing electric fields

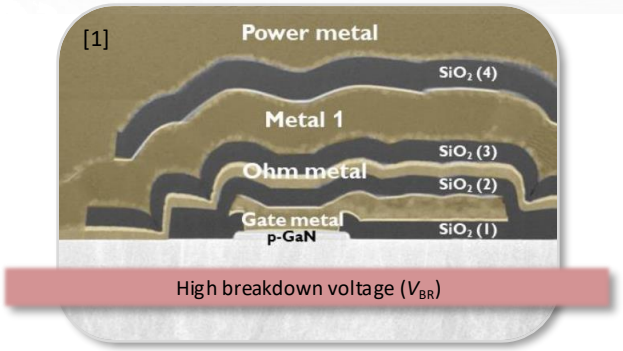
Challenges to increase the V_{BR}

Field plates are ubiquitous in lateral GaN HEMTs: by extending a metal plate (connected to gate or source) over the drain-side drift region, the peak field at the gate edge is reduced and the field is spread out more linearly, allowing a higher Vbr for the same channel-to-drain distance.

E field peaks at the gate edge, degrading the V_{BR}





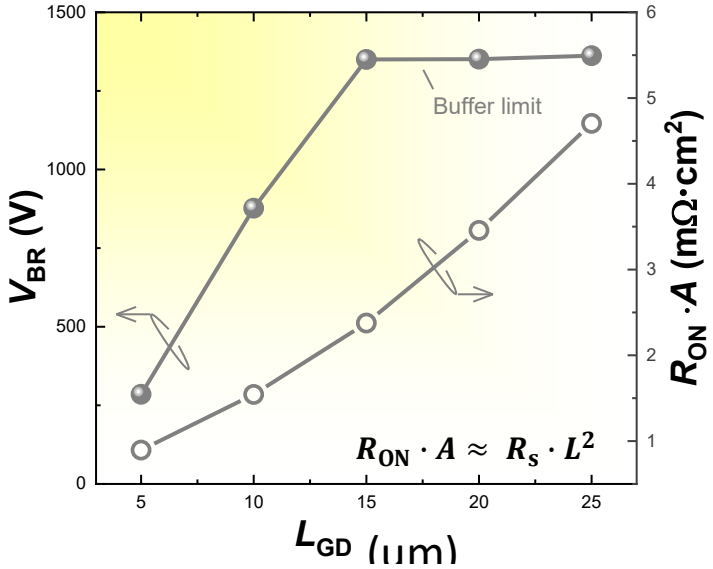


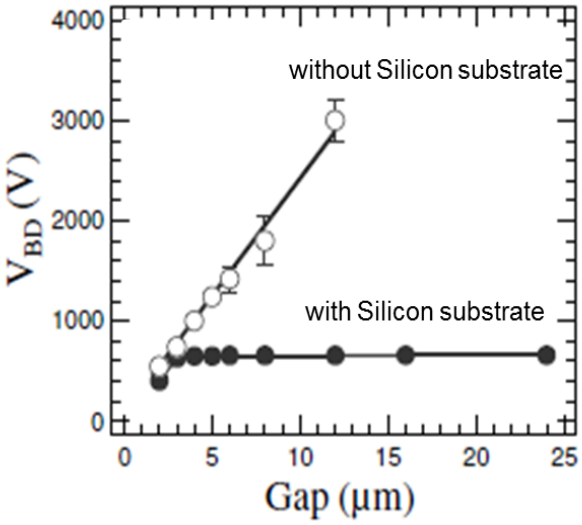
[1] IMEC, "Perspectives for disruptive 200 mm/8-inch GaN power device and GaN-IC technology," SEMICON Europa 2018.

There is a trade-off: field plates add to device capacitances (Cgd), which can increase switching loss. Thus, manufacturers optimize field plate dimensions to balance high VBR and fast switching.

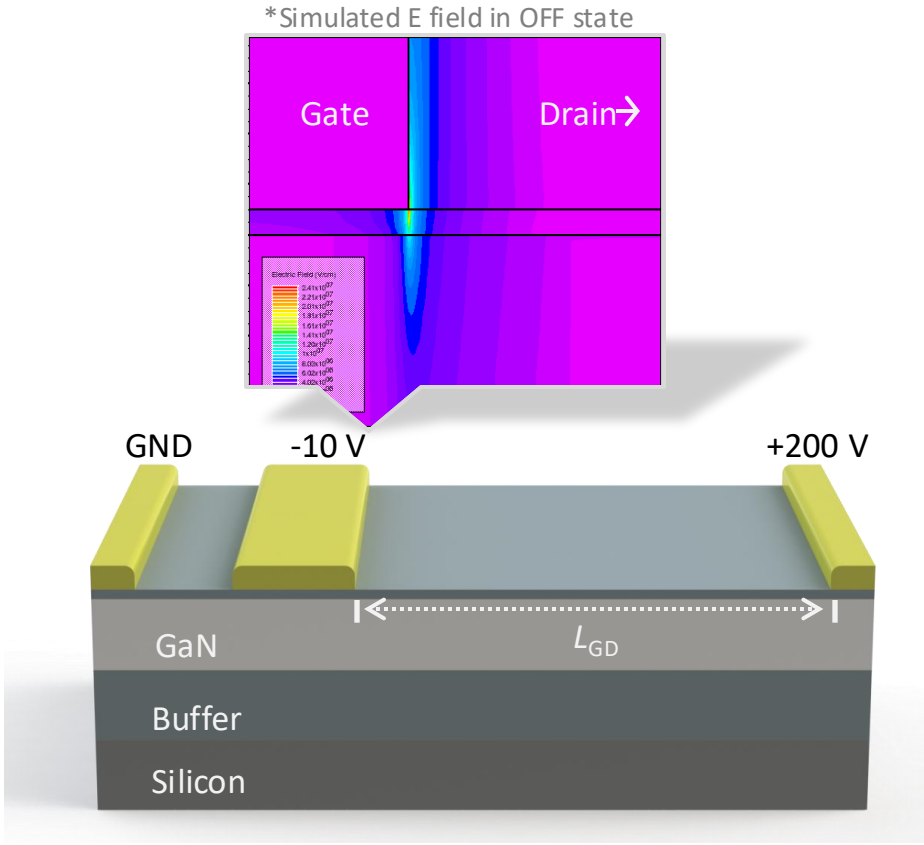
High V_{BR} at small L_{GD} for smaller R_{ON}·A

The electric field in lateral devices is not uniform and buffer limit the breakdown voltage





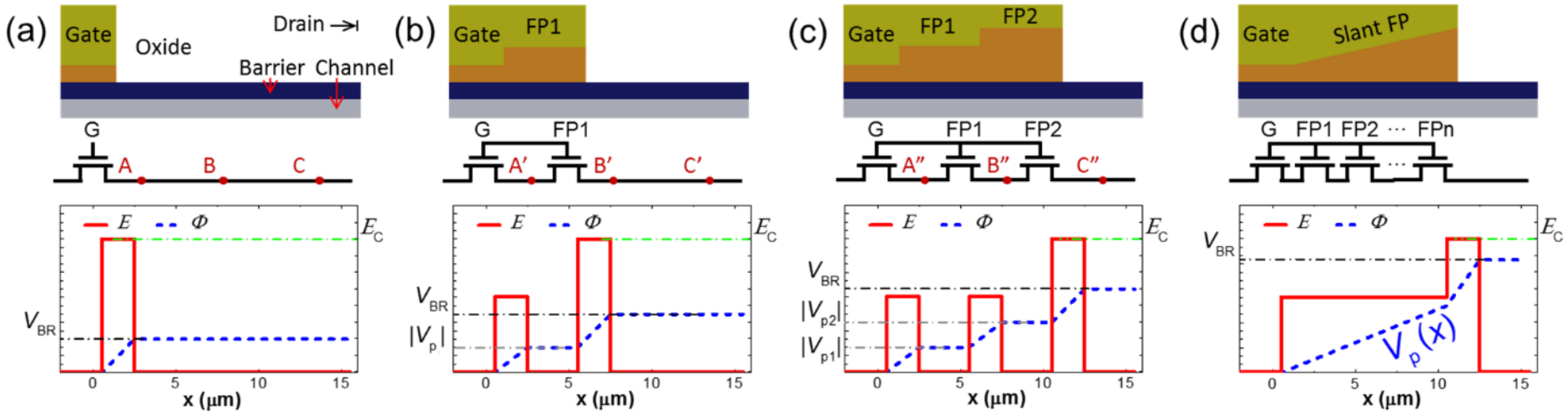
P. Srivastava, PhD thesis, 2012



The non-uniform E field degrades the V_{BR}

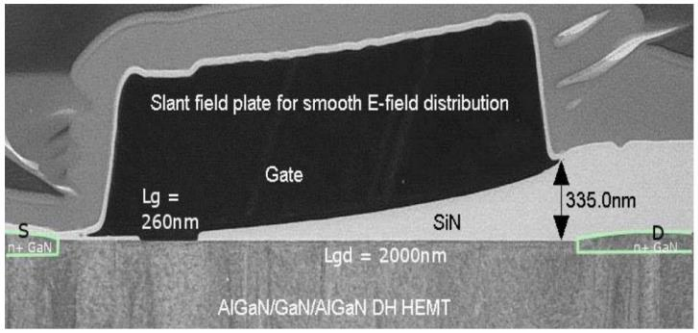
High V_{BR} at small L_{GD} for smaller R_{ON}-A

Electric field distribution in lateral device is inhomogeneous: limits the breakdown voltage

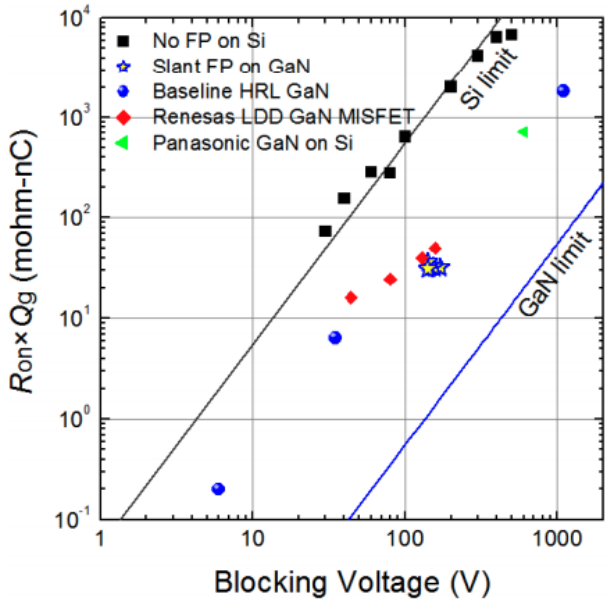


Slanted Field Plates:

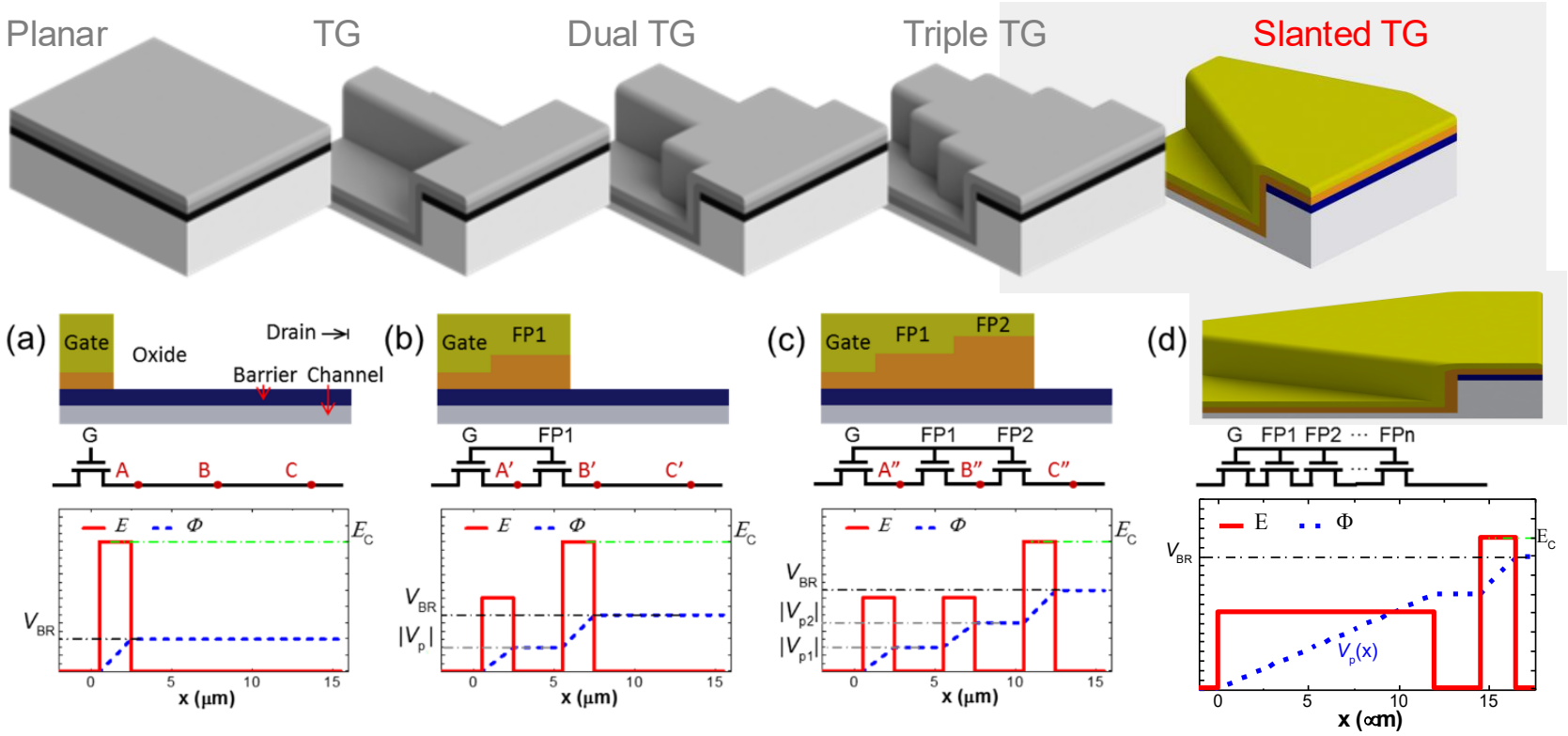
- Challenging design and difficult to control oxide thickness
- Limits the design flexibility of the field plates



[1] J. Wong, *et al*, IEEE EDL, 38, 95, 2017.



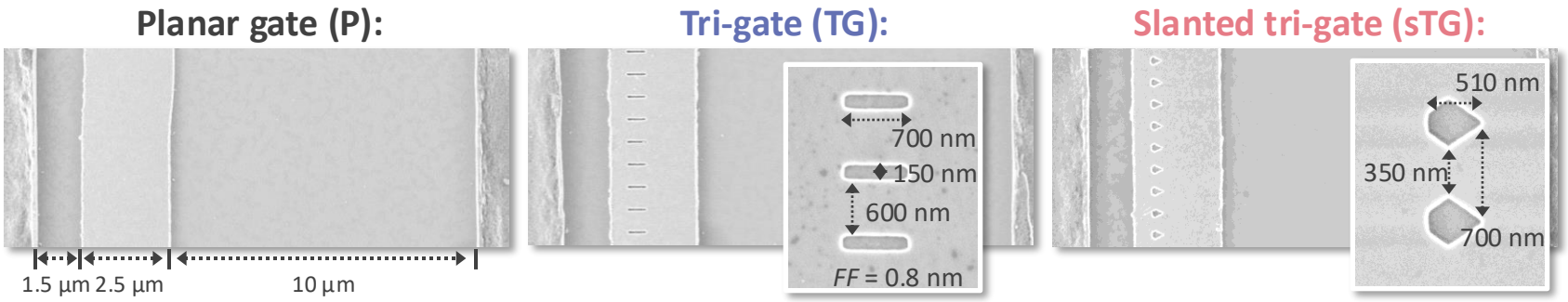
New concepts: Slanted tri-gates for high voltage devices

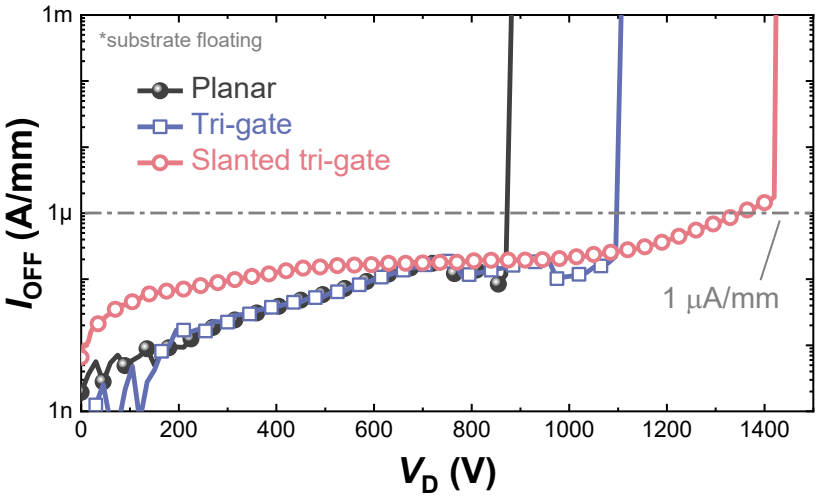


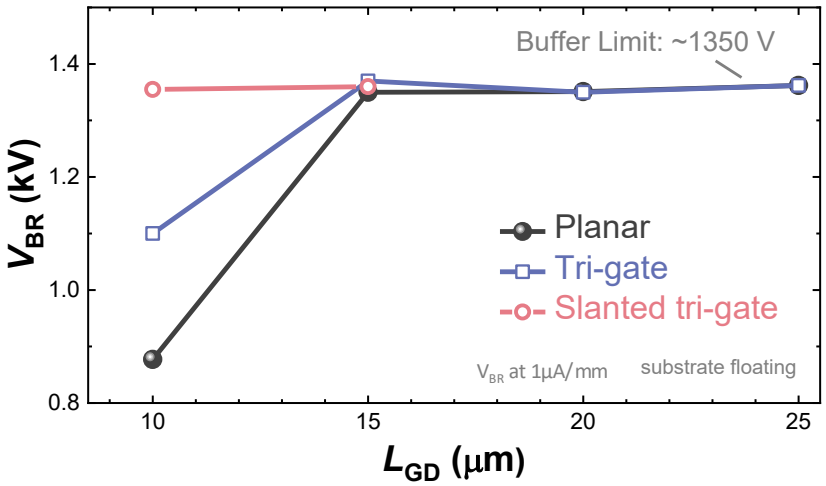
V_{th} can be engineered with tri-gate width:
Flexible design flexibility of field plates (with one lithography step)

J. Ma and E. Matioli, **IEEE Electron Device Letters** 38 (9), 1305-1308, **Jul. 2017**

New concepts: Slanted tri-gates for high voltage devices







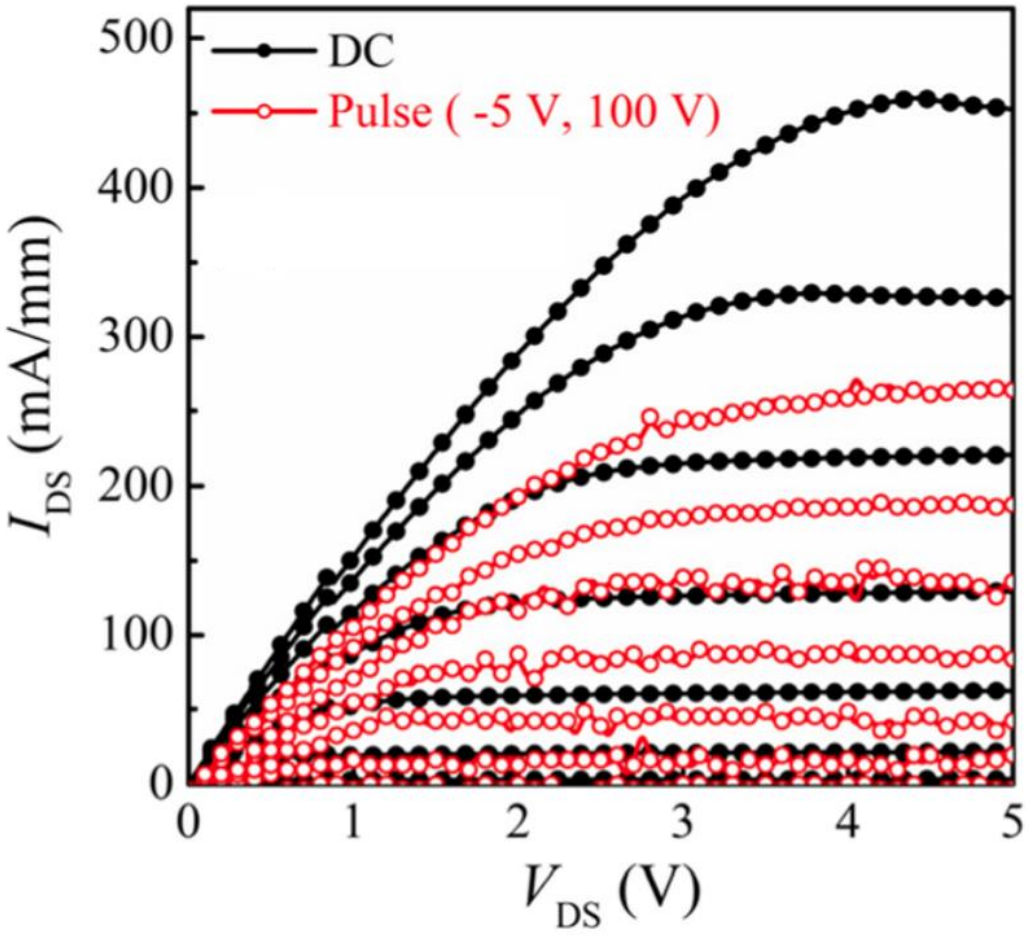
J. Ma and E. Matioli, **IEEE Electron Device Letters** 38 (9), 1305-1308, **Jul. 2017**

Enhanced V_{BR} & Reduced $R_{ON}{\cdot}A$ by the slanted tri-gate

Dynamic behavior of lateral devices

Current collapse and dynamic on-resistance: effect of trap states

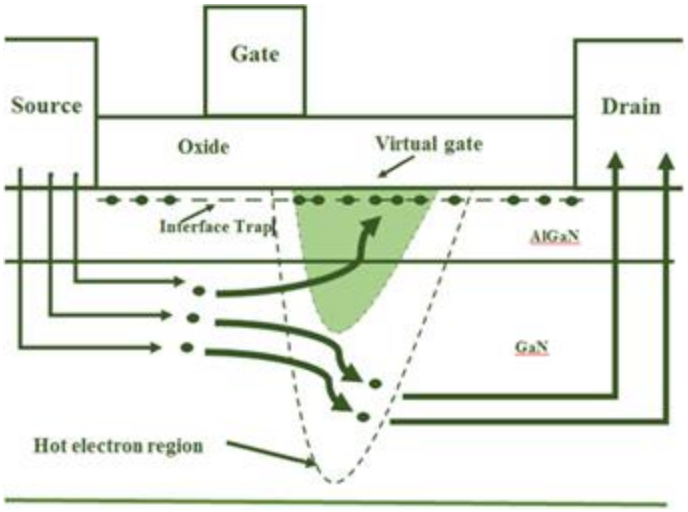
What is current collapse?



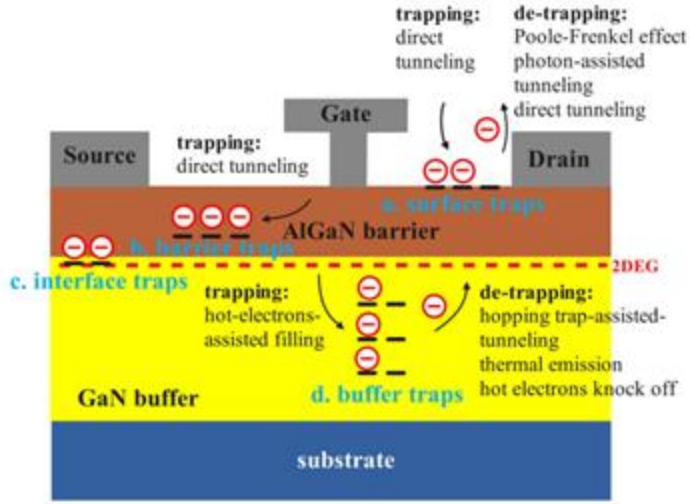
Current collapse and dynamic on-resistance: effect of trap states

The Reasons For Current Collapse

1. Surface Traps
2. Buffer Traps
3. Hot Electron Injection
4. Interface Traps
5. Barrier Traps

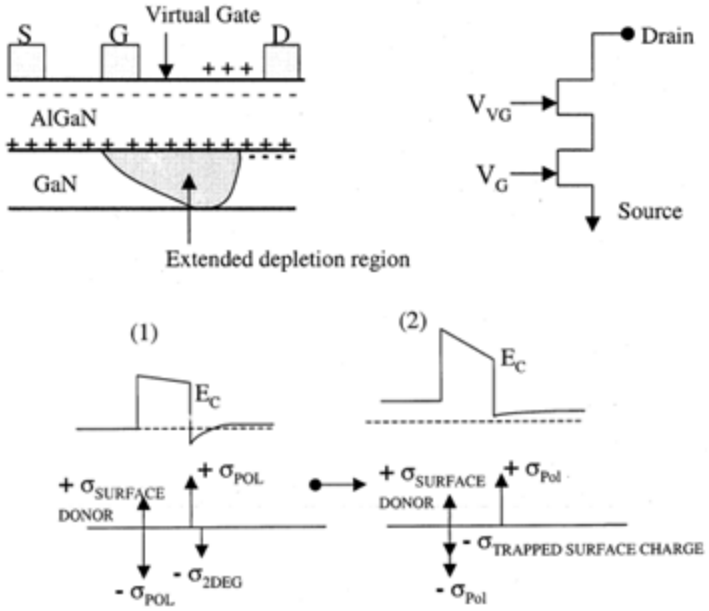


Trapping Mechanisms
P. Kharei, A. Baidya, N. P. Maity, and R. Maity, "An insight to current collapse in Gan HEMT and suppressing techniques," *Engineering Research Express*, vol. 5, no. 1, p. 012001, Jan. 2023. doi:10.1088/2631-8695/acb131



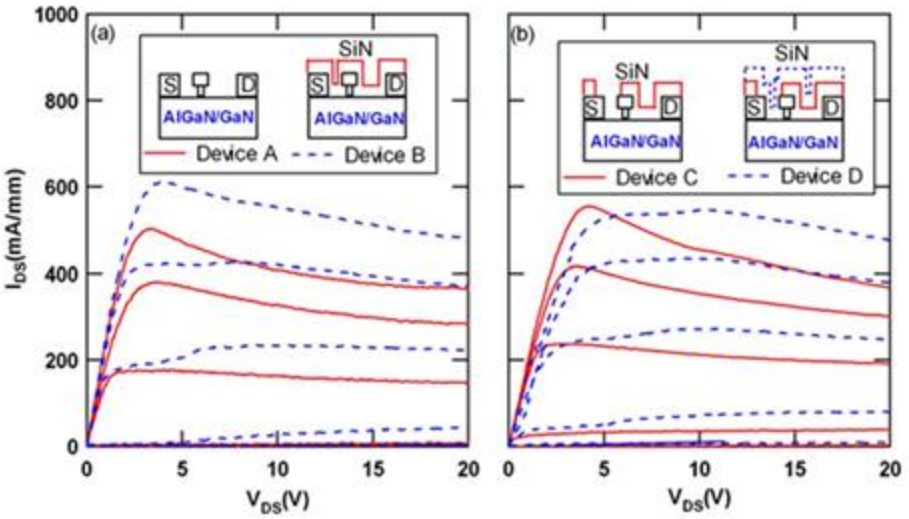
Main Trapping Mechanisms
R. Ye *et al.*, "An Overview on Analyses and Suppression Methods of Trapping Effects in AlGaN/GaN HEMTs," in *IEEE Access*, vol. 10, pp. 21759-21773, 2022, doi: 10.1109/ACCESS.2021.3139443.

Current collapse and dynamic on-resistance: effect of trap states



Virtual Gate

R. Vetury, et al. *IEEE Transactions on Electron Devices*, vol. 48, no. 3, pp. 560-566, March 2001



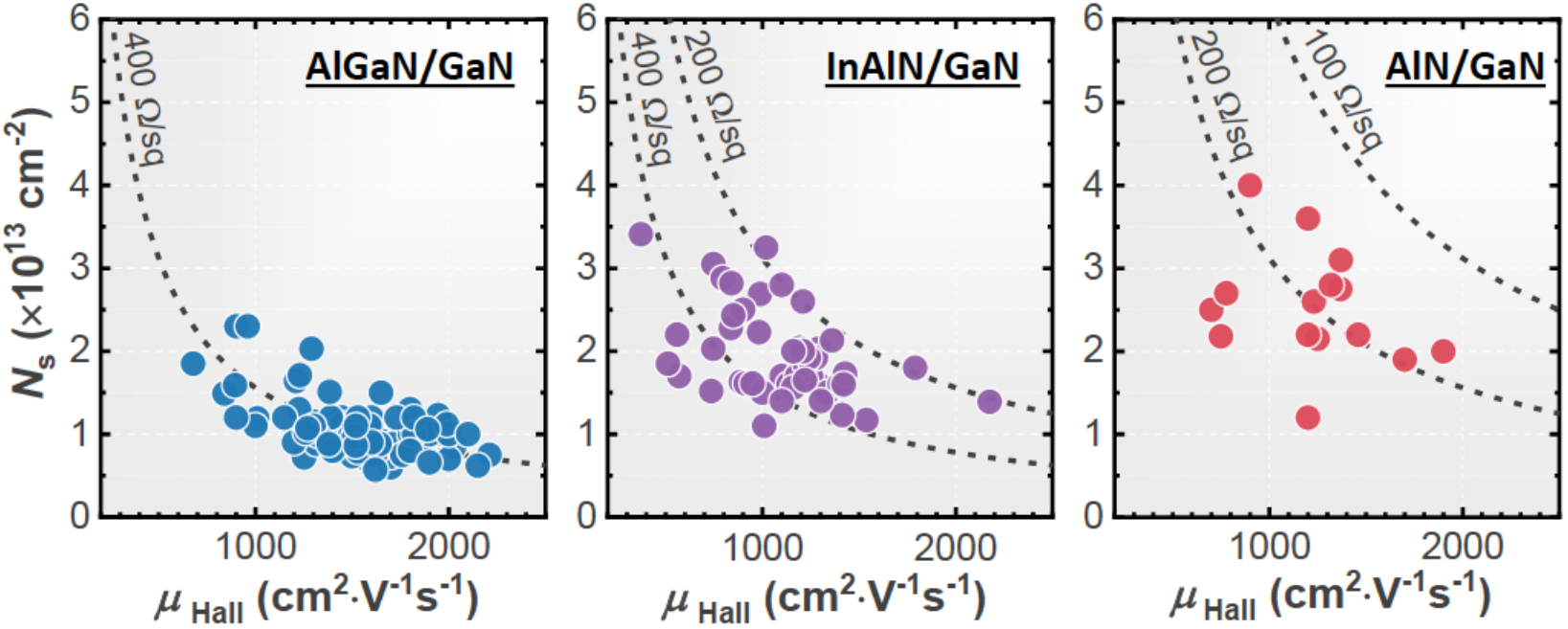
Passivation for Surface Charges

S. Arulkumaran et al. *Applied Physics Letters*, vol. 90, no. 17, Apr. 2007. doi:10.1063/1.2730748

Advanced concept : Reaching ultra low on-resistance

Reducing sheet resistance

Intrinsic trade-off: increasing n_s deteriorates μ

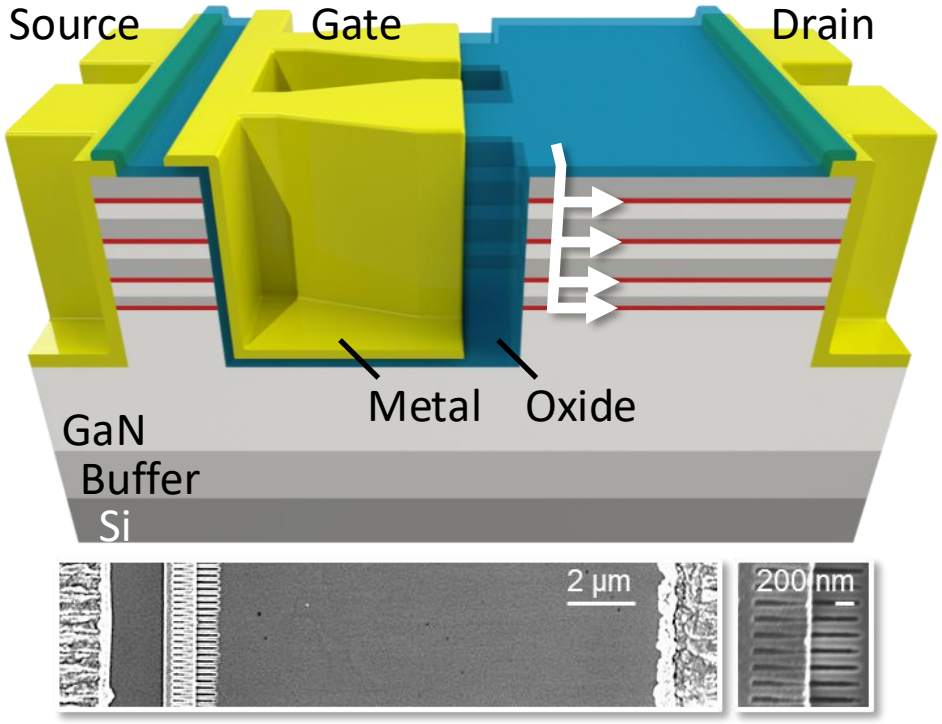


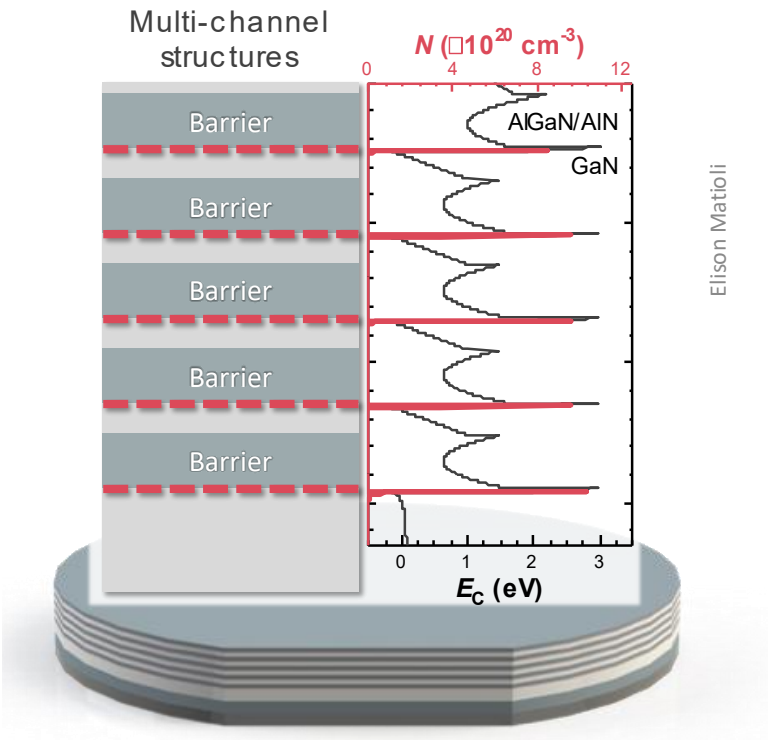
Low sheet resistance (R_{sh}) requires both high n_s and high μ

Elison Matioli

Multichannel power devices

Our approach: Multiple 2DEG channels





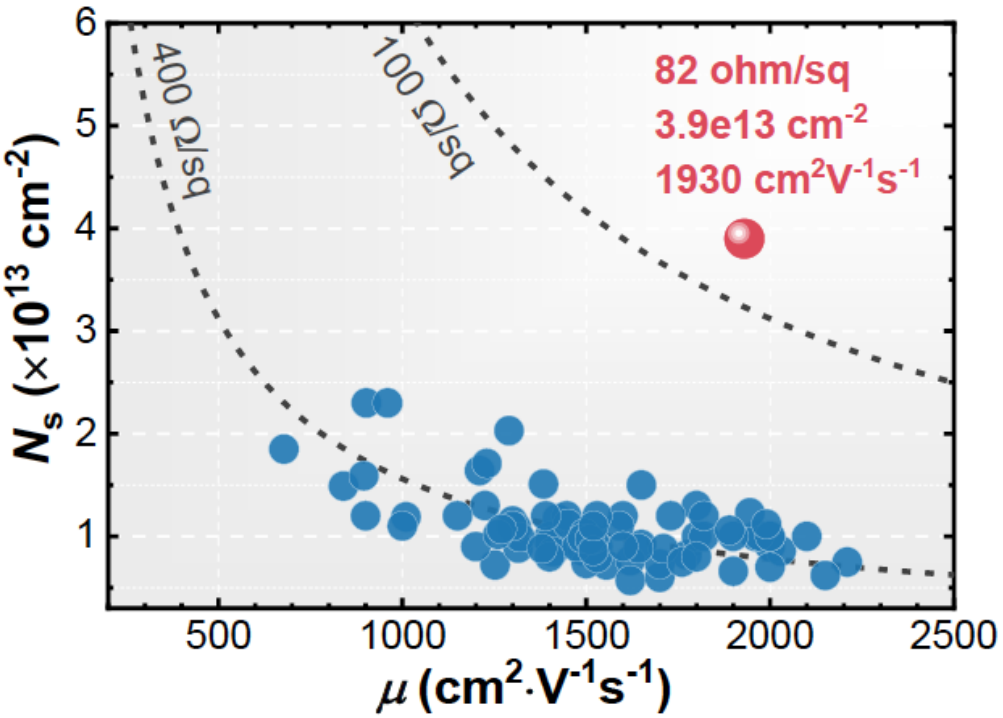
Elison Matioli

J. Ma, C. Erine, P. Xiang, K. Cheng and E. Matioli, **APL**, 113, 24, 242102, 2018
J. Ma, C. Erine, M. Zhu, L. Nela, P. Xiang, K. Cheng and E. Matioli, IEEE **IEDM** 2019
L. Nela, J. Ma, C. Erine, P. Xiang, T.-H. Shen, V. Tileli, T. Wang, K. Cheng, E. Matioli, **Nature Electronics**, *Mar. 2021*

Multichannel power devices

Multi-channel: high μ and high Ns

4-times higher n_s than in single-channel AlGaN/GaN, together with high mobility



Single-channel:

AlGaN barrier

Multi-channel:

This work (AlGaN barriers)

*Only Hall results are included

Other barriers are also possible:

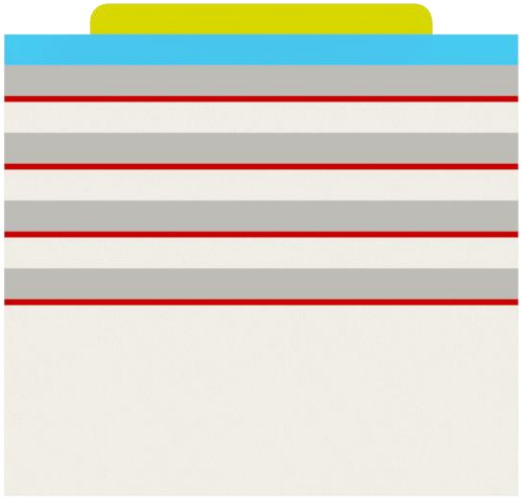
AlN/GaN (10x-channels): 128 ohm/sq (CORNELL): Y. Cao, et al., J. Cryst. Growth 323, 529 (2011).

InAlN/GaN (10x-channels) 36 ohm/sq (our group): P Sohi et al 2021 Semicond. Sci. Technol. 36 055020 (2021)

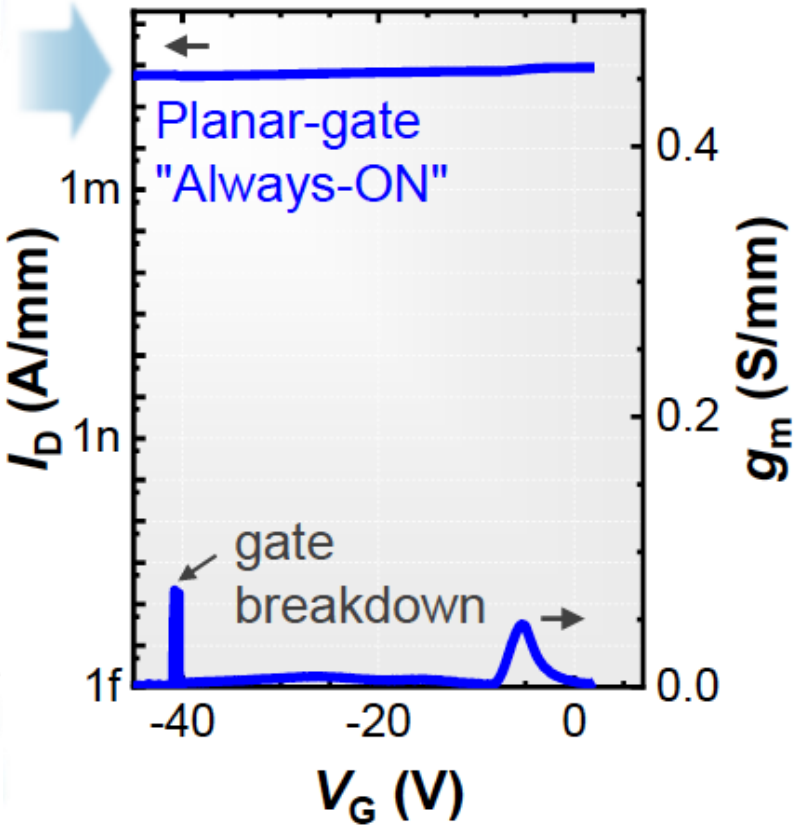
Tri-gates are unique to control multi-channels

Low R_{Sh} is useless if the channels cannot be controlled

Planar gate



Poor electrostatic control
Channels controlled one by one



Tri-gates are unique to control multi-channels

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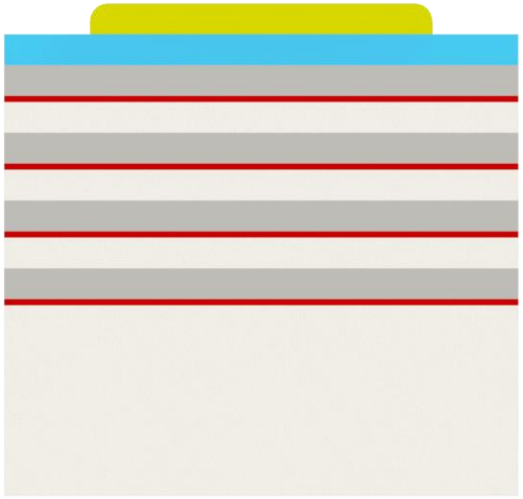

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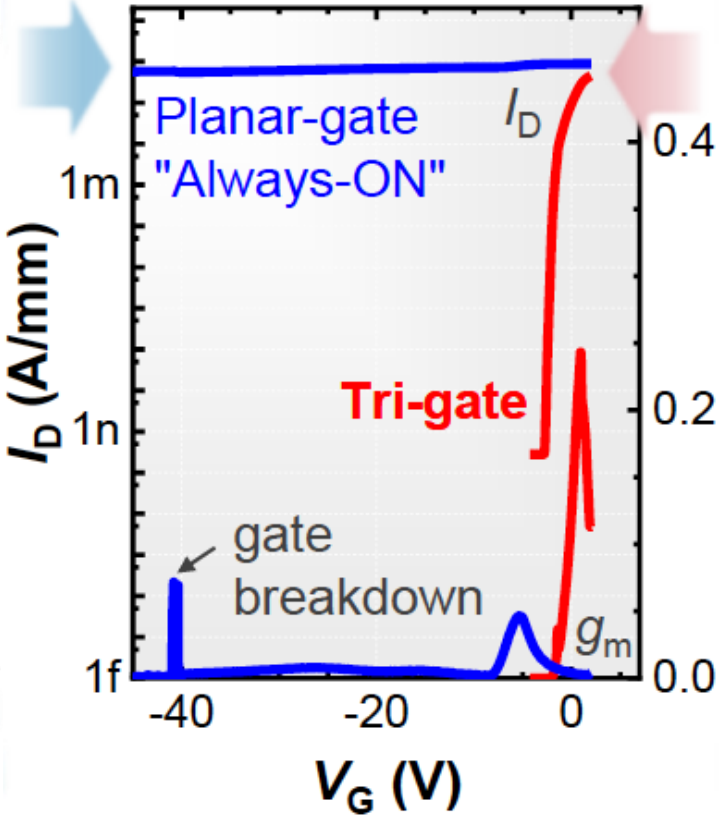
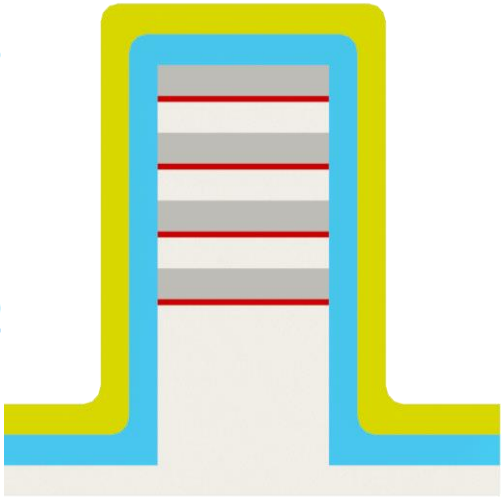


Tri-gate



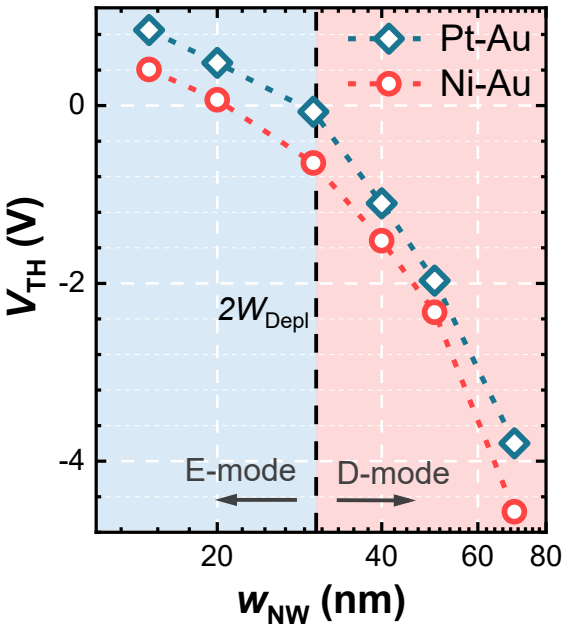
Excellent 3D tri-gate control
Simultaneous control

Elison Matioli

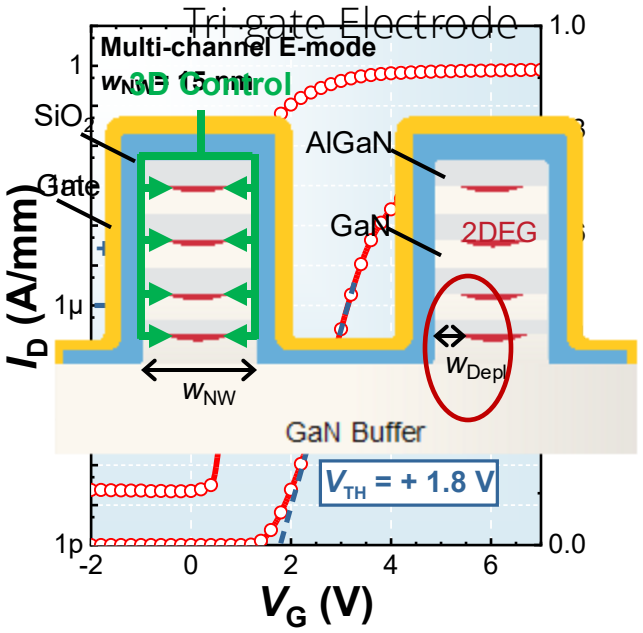
Multichannel power devices

E-mode operation with high work-function gate metal

High work-function gate metal



Full E-mode operation



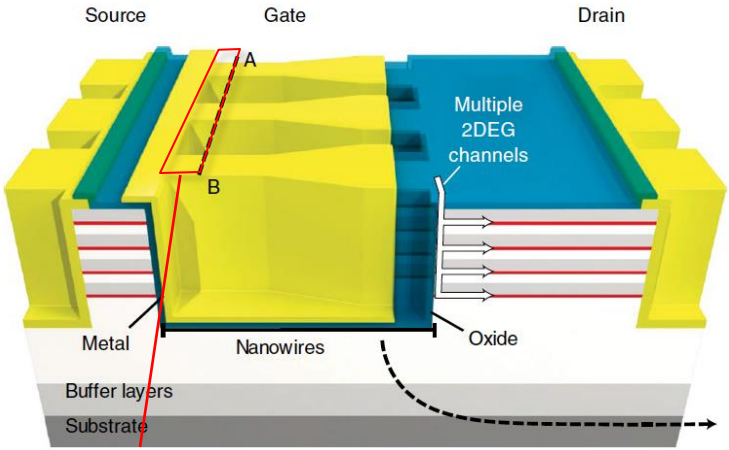
Full e-mode operation can be achieved despite the large n_s

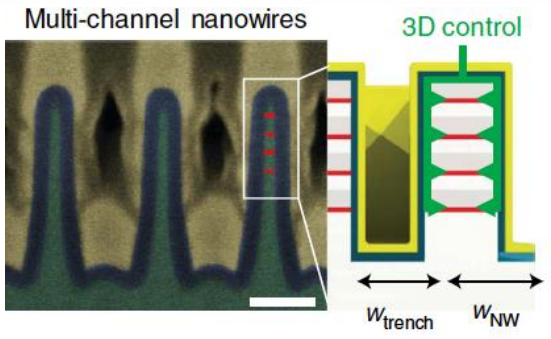
L Nela, M Zhu, J Ma, E Matioli, **IEEE Electron Device Letters,** 40 (3), 439-442 2019

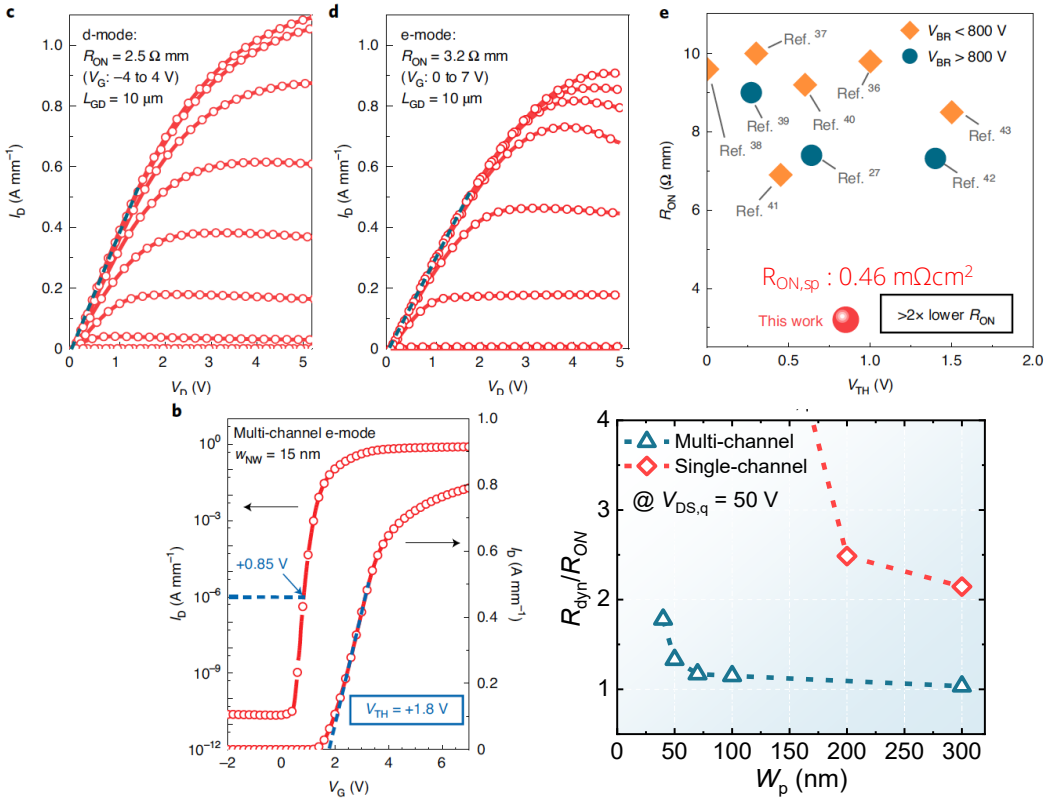
L. Nela, J. Ma, C. Erine, P. Xiang, T.-H. Shen, V. Tileli, T. Wang, K. Cheng, E. Matioli, **Nature Electronics**, Mar. 2021

Multichannel power devices

Multi-channel control: Tri-gates are unique solution





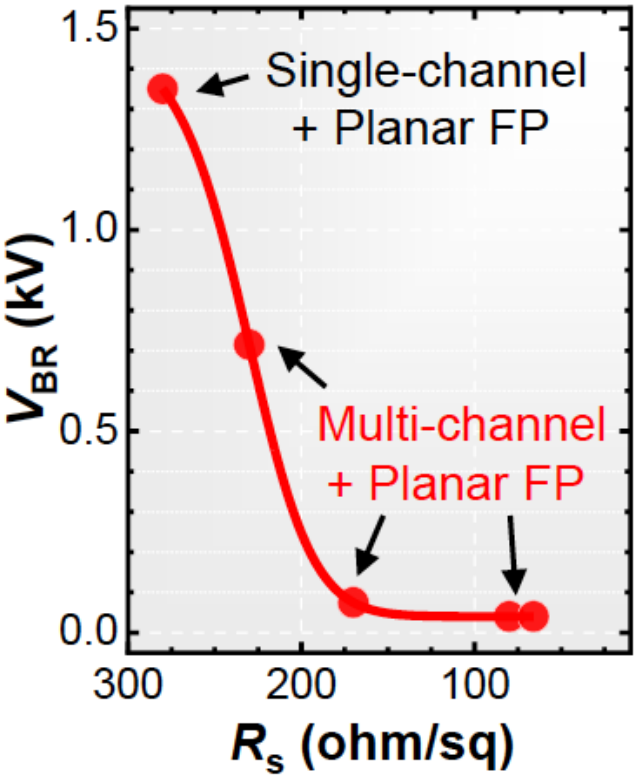


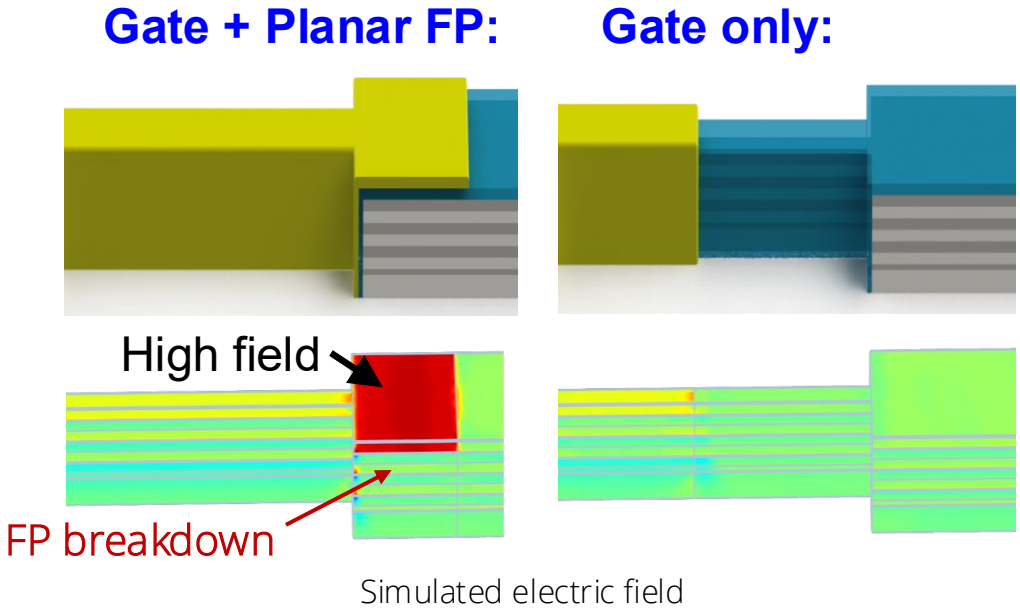
L. Nela, J. Ma, C. Erine, P. Xiang, T.-H. Shen, V. Tileli, T. Wang, K. Cheng, E. Matioli, **Nature Electronics**, Mar. 2021
L. Nela; H. K. Yildirim; C. Erine; R. Van Erp; P. Xiang; K. Cheng; E. Matioli, **IEEE Electron Device Letters** (2020)

Multichannel power devices

Issue of high breakdown voltage in multichannels

2D Field Plates are NOT suited for high conductivity channels





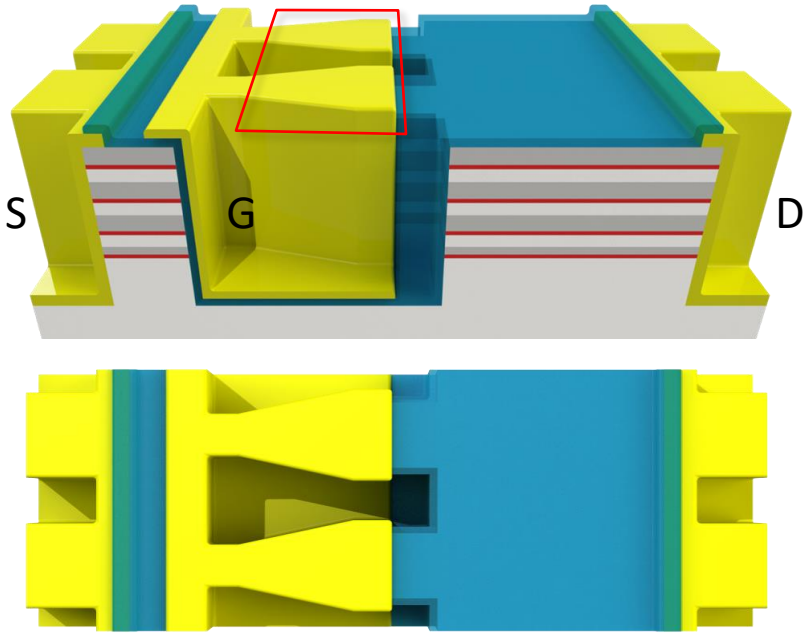
Simulated electric field

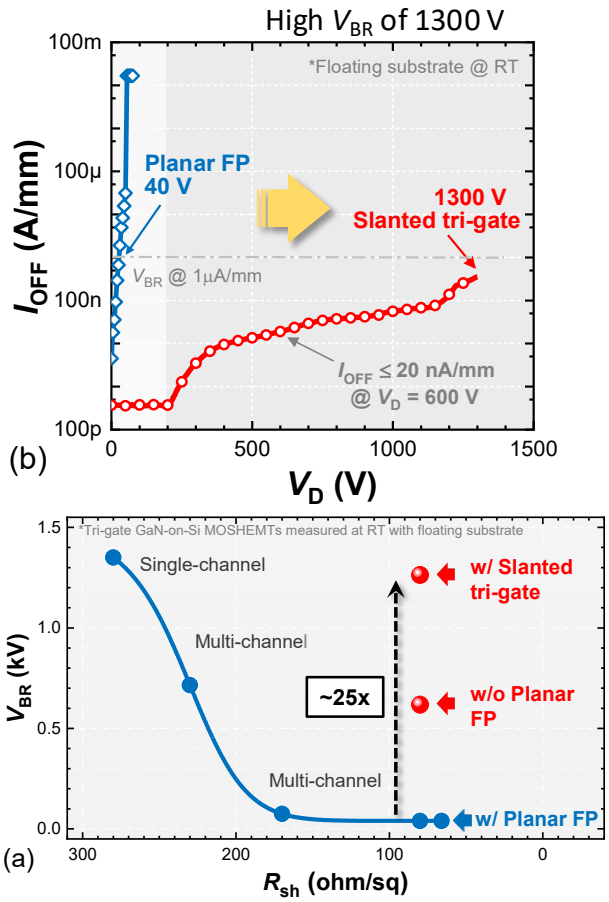
3D Field Plates are needed
for high-conductivity multi-channels

J. Ma, C. Erine, M. Zhu, L. Nela, P. Xiang, K. Cheng and E. Matioli, **IEDM** 2019

Slanted tri-gate termination for multichannel devices

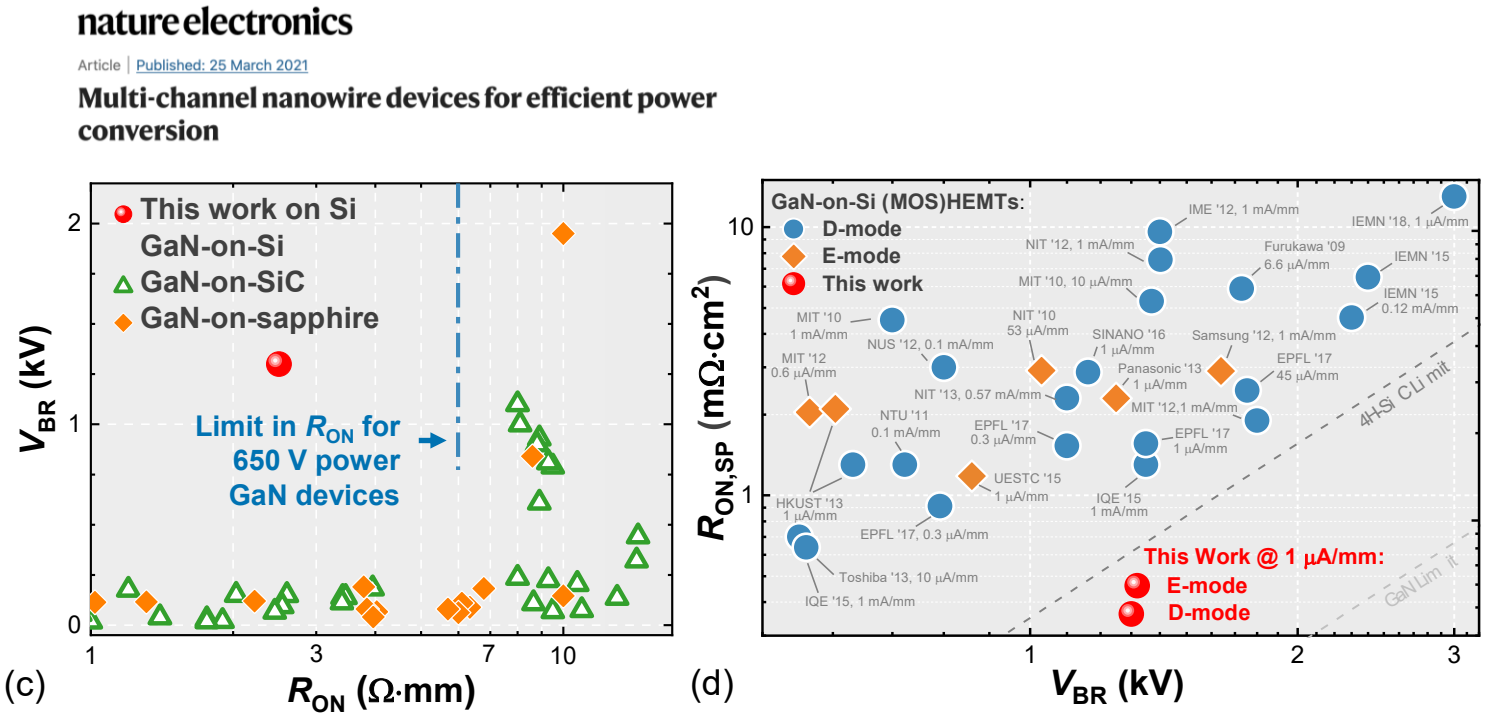
Slanted tri-gates for high breakdown voltage





L. Nela, J. Ma, C. Erine, P. Xiang, T.-H. Shen, V. Tileli, T. Wang, K. Cheng, E. Matioli, **Nature Electronics**, *Mar. 2021*

Multichannel power devices



FOM: 4.6 GW/cm^2 for d-mode devices and 3.8 GW/cm^2 for e-mode devices

Tri-gate + multi-channels:
Promising pathway for efficient power electronic devices

L. Nela, J. Ma, C. Erine, P. Xiang, T.-H. Shen, V. Tileli, T. Wang, K. Cheng, E. Matioli, **Nature Electronics**, *Mar. 2021*