GaN electronic devices

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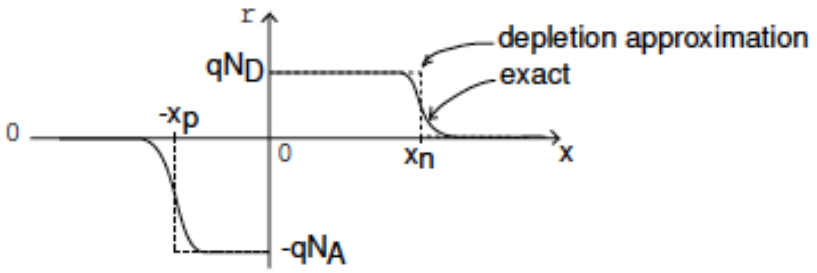
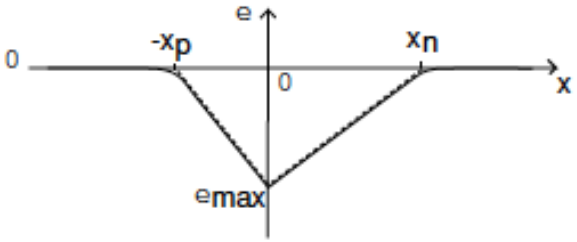
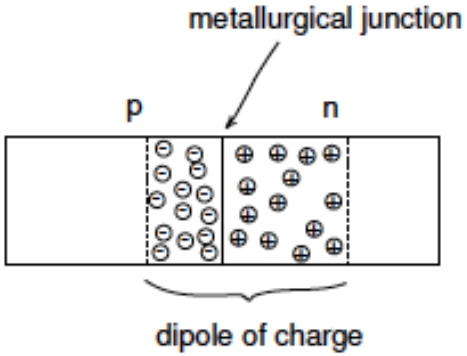
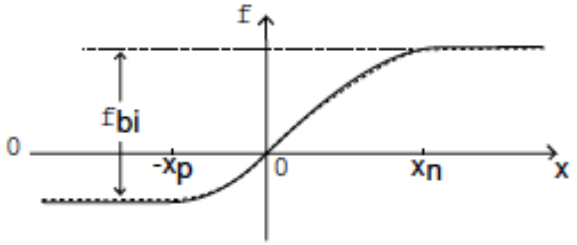
Vertical GaN devices

Back to pn junctions





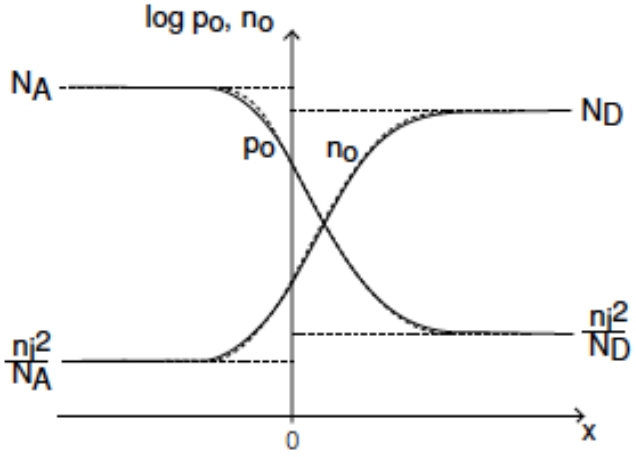




Distinct regions:
Around metallurgical junction:
space charge region (SCR)

Far from junction:
quasi-neutral regions (QNR)
ρ ~ 0

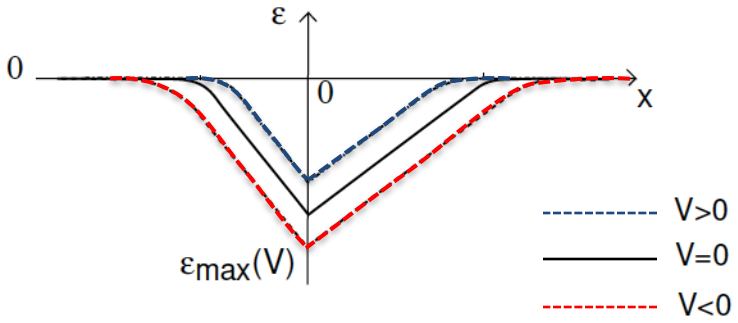
Electric field is constant and equal to zero

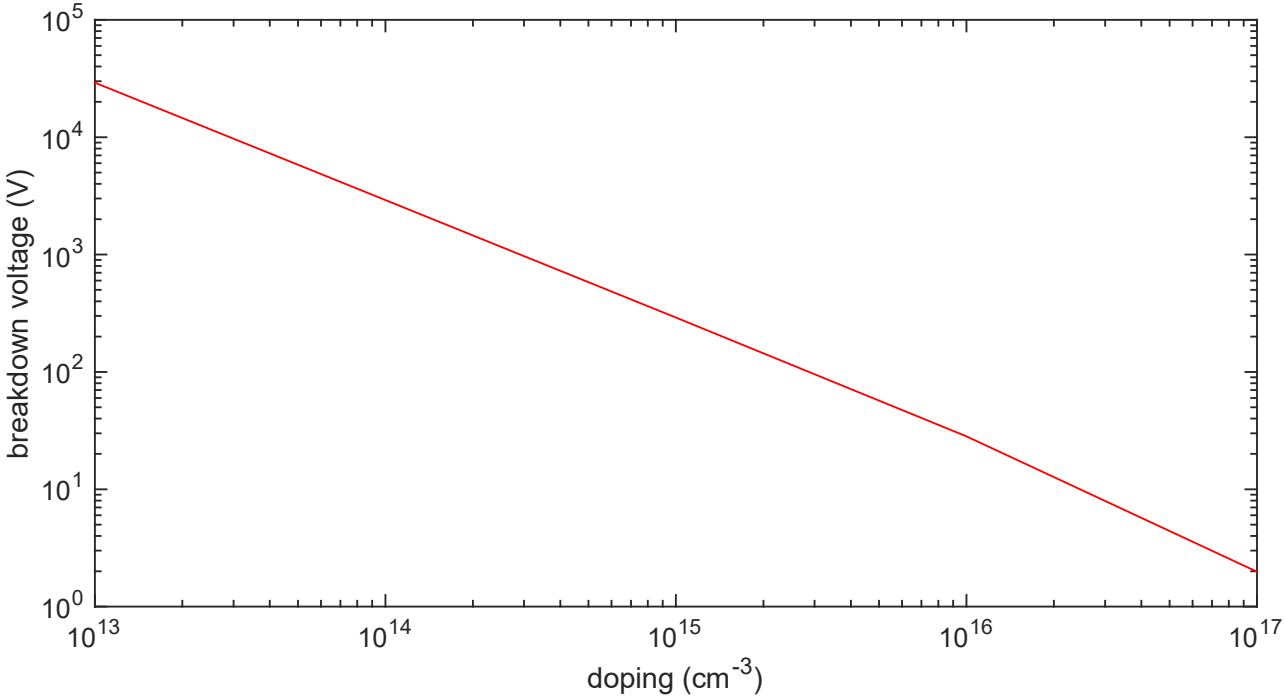


Ideal p-n junction out of equilibrium

Peak electric field:

$$|\mathcal{E}_{max}(V)| = \sqrt{\frac{2qN_AN_D(\phi_{bi}-V)}{\epsilon(N_D+N_A)}} = |\mathcal{E}_{max}(V=0)|\sqrt{1-\frac{V}{\phi_{bi}}}$$





How to make a power device?

Power diodes

Goal:

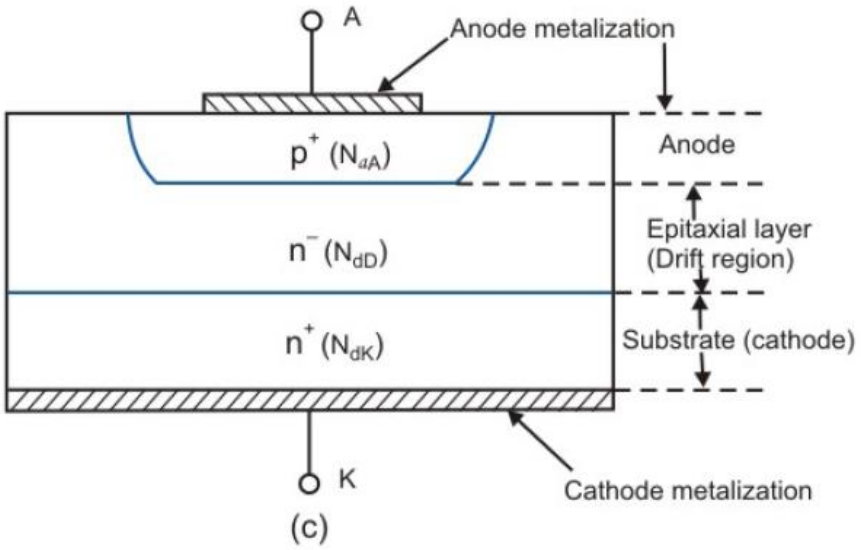
Conduct **several kilo amps** of current in the forward direction with very **little power loss** while blocking **several kilo volts** in the reverse direction.

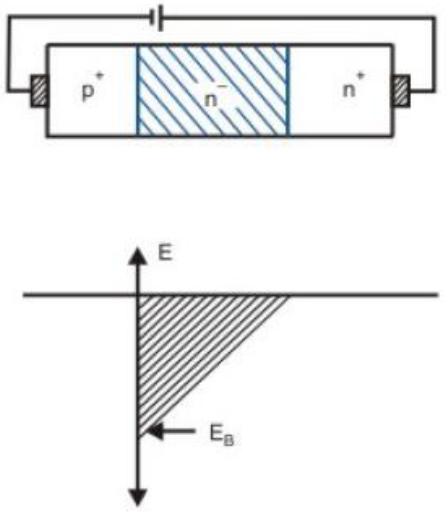
Large blocking voltage requires **wide depletion layer** in order to restrict the maximum electric field strength below the breakdown voltage (impact ionization level).

Space **charge density in the depletion layer should also be low** in order to yield a wide depletion layer for a given **maximum electric field strength**.

This is satisfied in a **lightly doped p-n junction** diode **of sufficient width** to accommodate the required depletion layer.

PIN diode



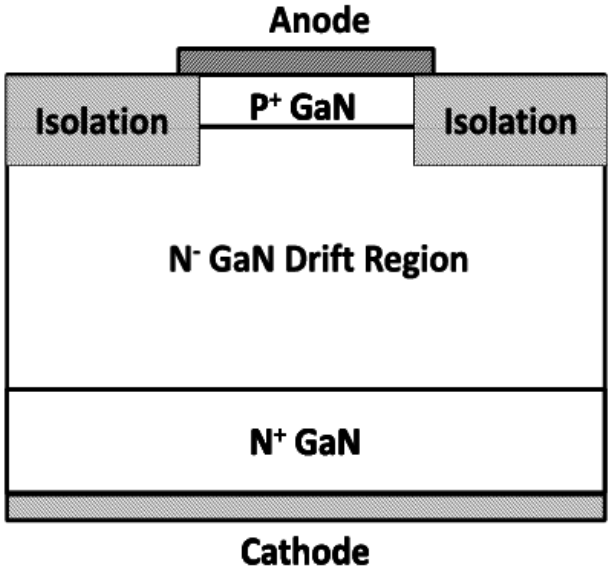


GaN Power PiN diodes

PIN diodes **on bulk GaN**

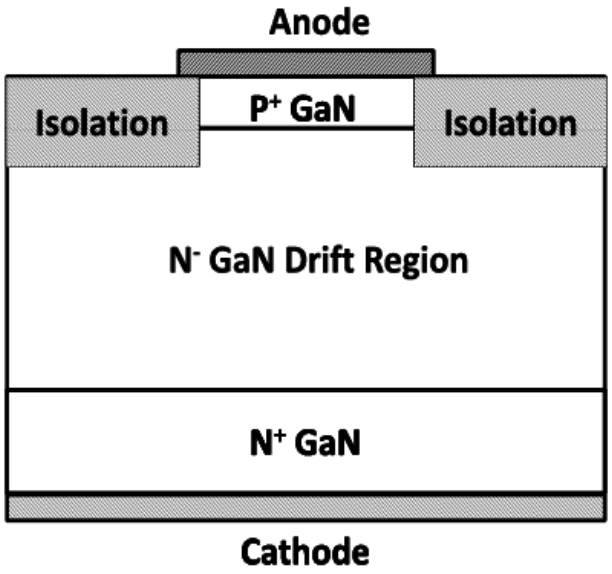
Pro:
Bulk GaN eliminates lattice mismatch and allows growth of much thicker drift layers
Low dislocation densities 10^4–10^6 cm^{-2} (however still much higher than those of Si and SiC substrates)

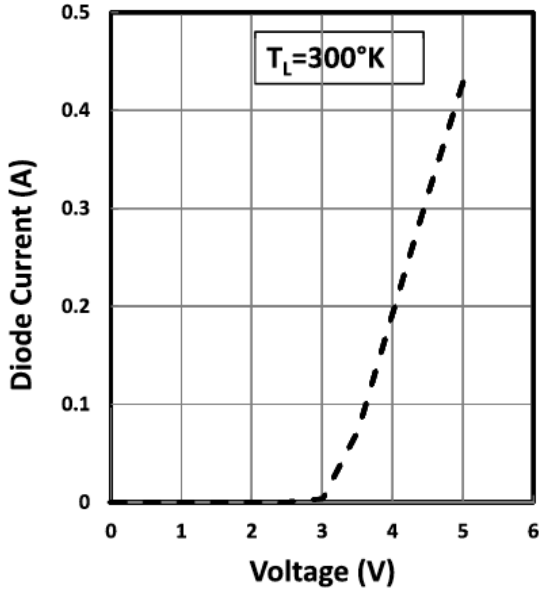
Cons:
Small size (2–3 inch size) and relatively high cost (100 euro/cm2) of the GaN substrates, compared to 4–6 inch wafer size and reasonable cost (<10 $/$cm^2$) of SiC

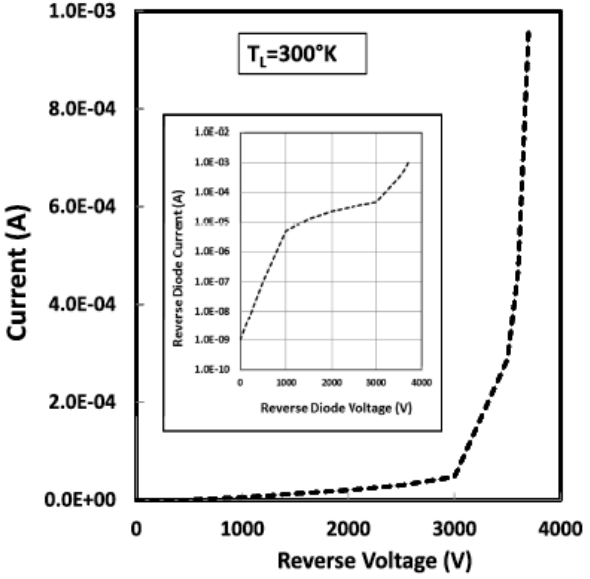


GaN Power PiN diodes

PIN diodes **on bulk GaN** (30 um drift layer)







- Drift region:
  - $N_D \approx 5 \times 10^{15}$ cm−3
  - **drift layer thicknesses are > 30µm.**
- Specific on-resistance of 2.95 mohm -cm2
- Breakdown voltages of 3.7 kV

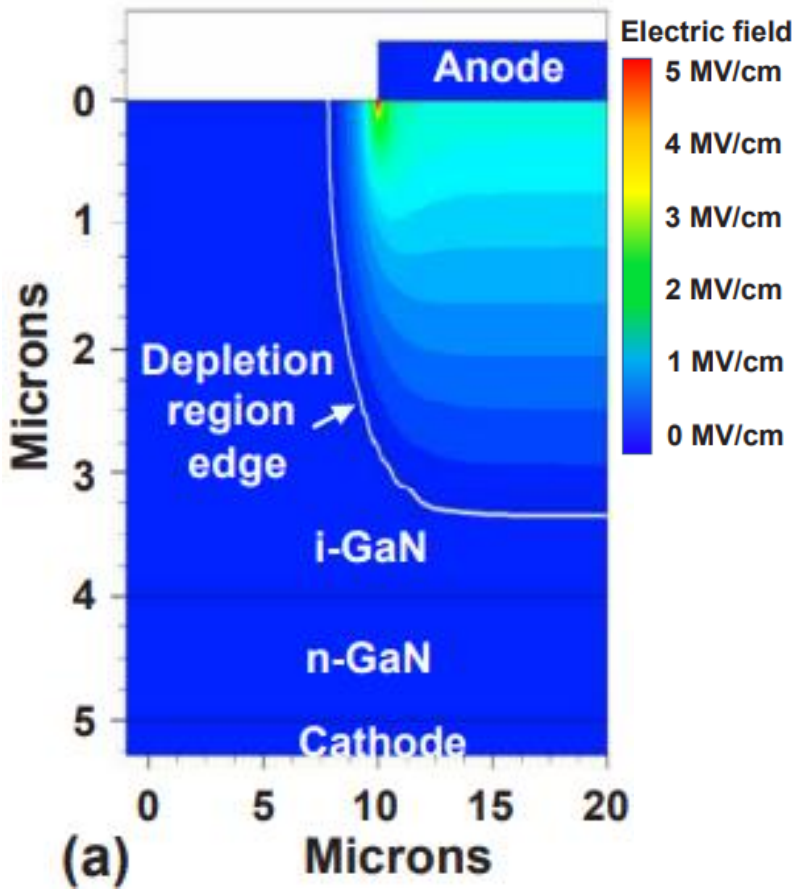
Avogy: Isik C. Kizilyalli et al., "3.7 kV Vertical GaN PN Diodes", IEEE ELECTRON DEVICE LETTERS, VOL. 35, NO. 2, FEBRUARY 2014

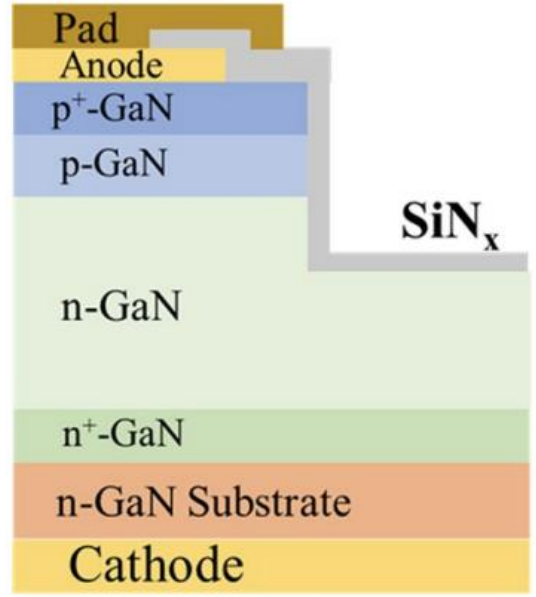
GaN Power PiN diodes

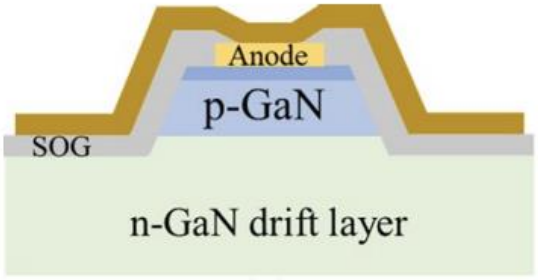
Field plates

High E at Schottky interface

High reverse leakage current

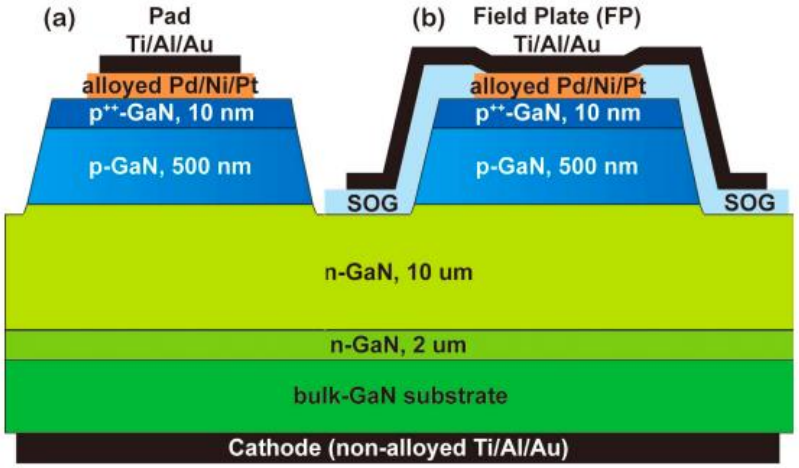


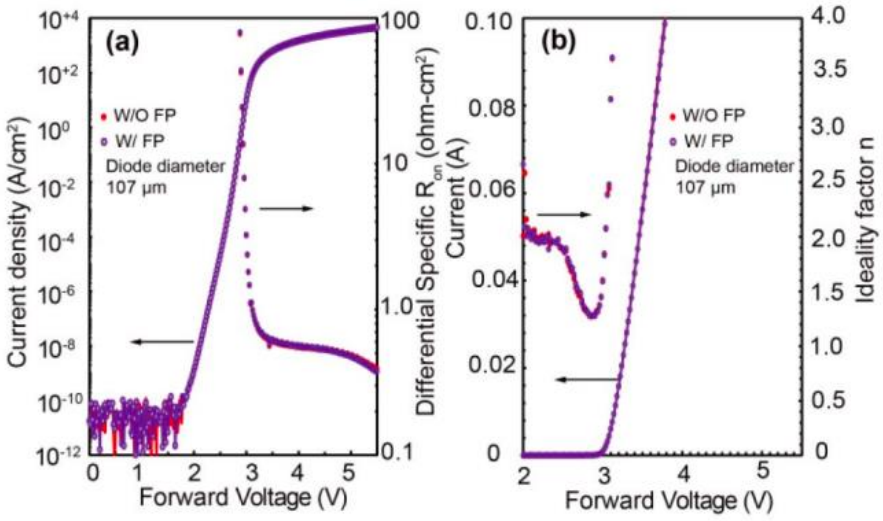


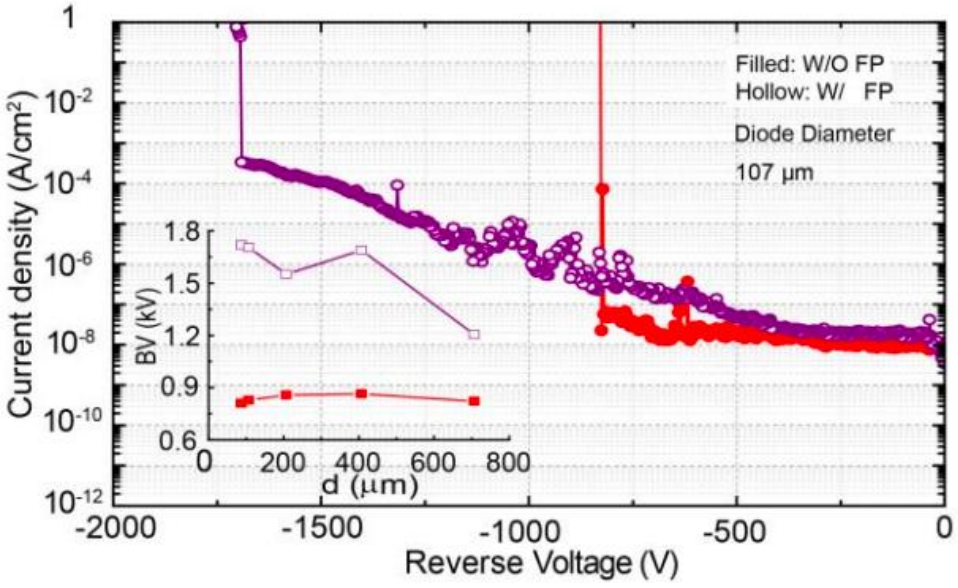


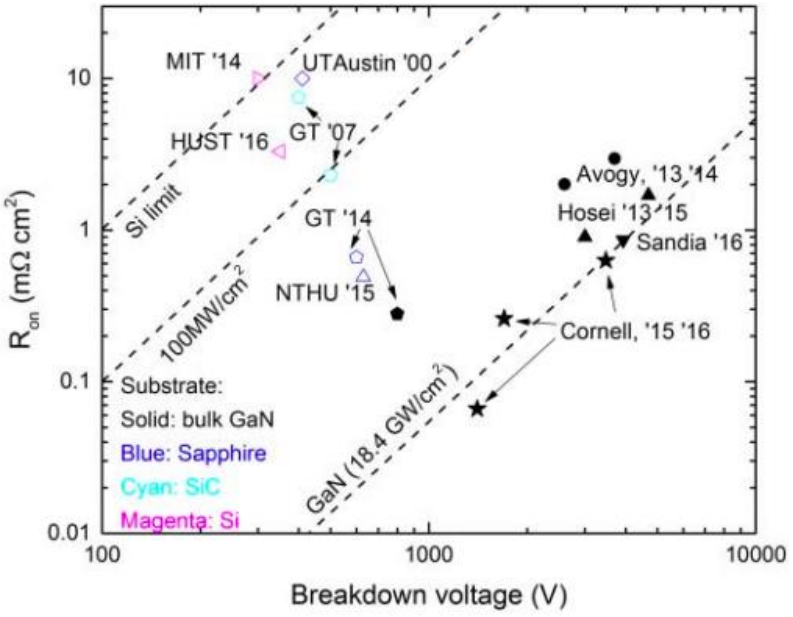
GaN Power PiN diodes

PIN diodes on bulk GaN (10 um drift layer)





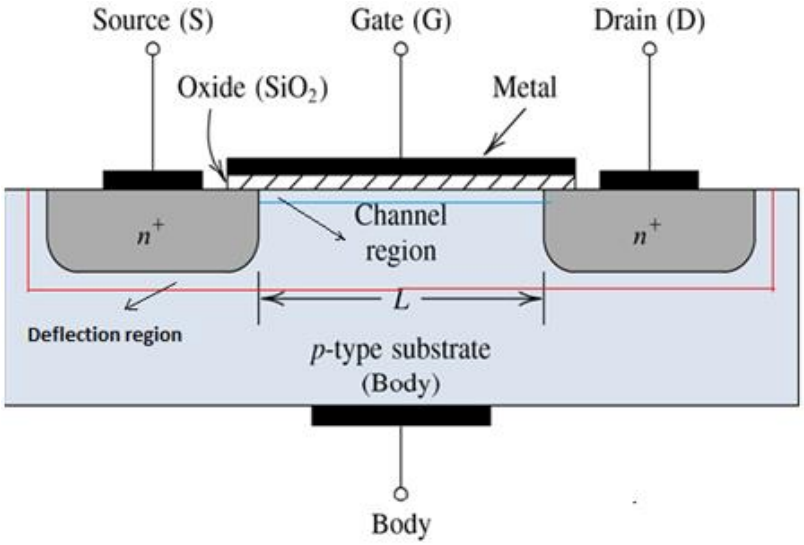




CORNELL: Kazuki Nomoto et al., IEEE ELECTRON DEVICE LETTERS, VOL. 37, NO. 2, FEBRUARY 2016

MOSFETs

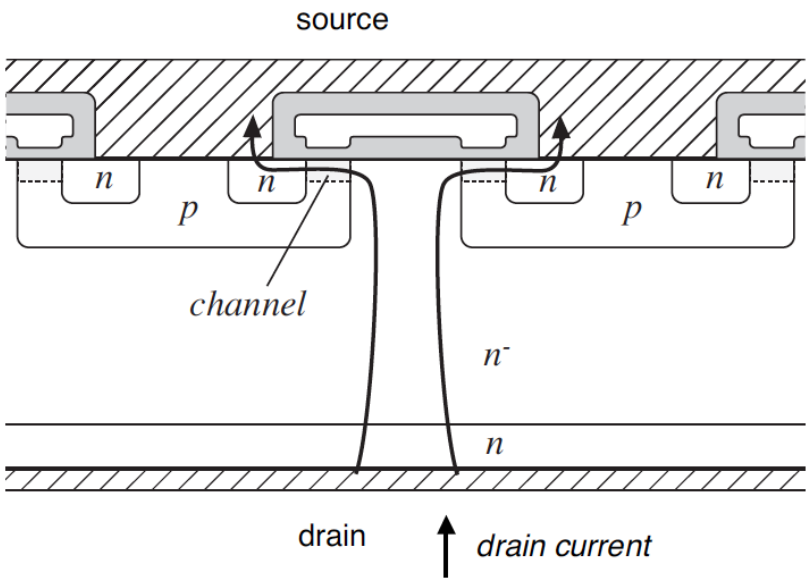
Lateral MOSFETs



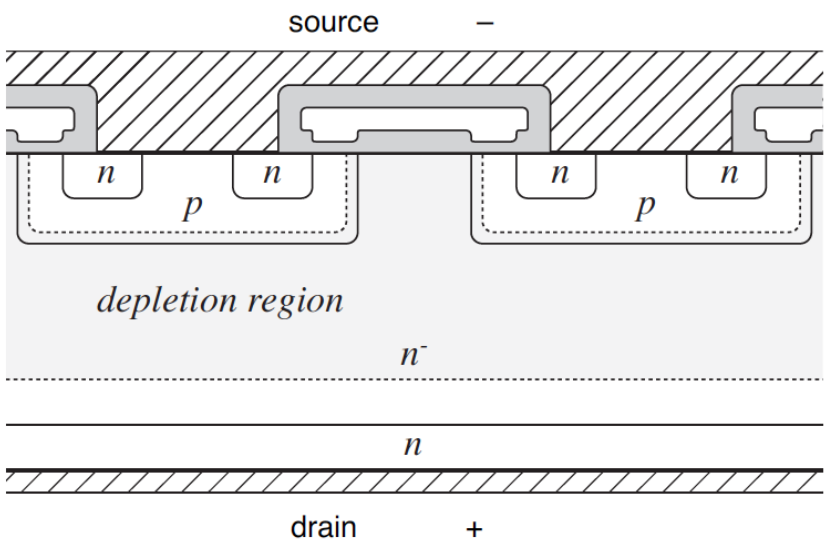
How to make vertical MOSFET?

Case of Silicon

Forward polarization: $V_{gs} > 0$



Reverse polarization: $V_{gs} < 0$



There are no minority carriers to cause conductivity modulation:

MOSFETs are majority carrier devices

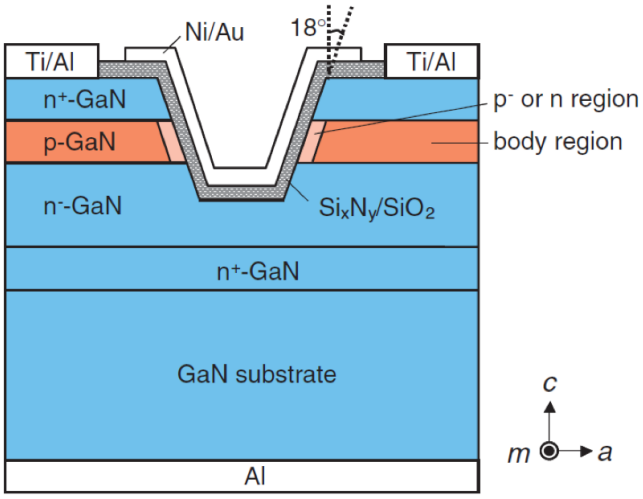
- Breakdown voltage is increased
- On-resistance dominated by resistance of n^- region (drift region)

Reverse polarization:
p-n and p-n^- reverse-biased:
voltage drops across n^- region

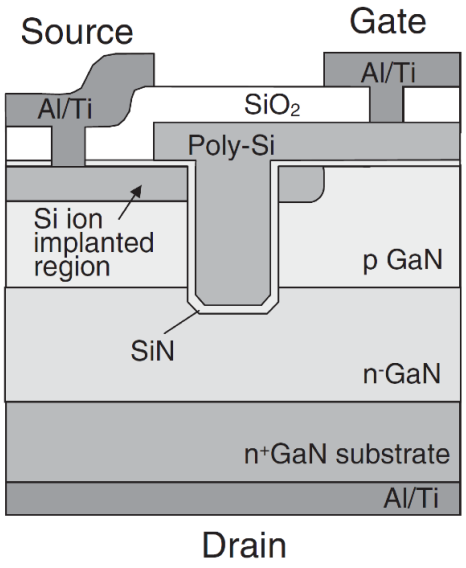
Fundamentals of Power Electronics, Robert W. Erickson, Dragan Maksimović

GaN vertical transistors

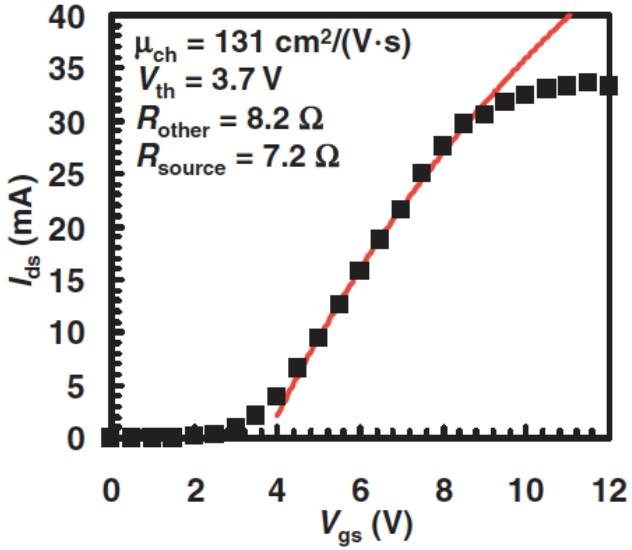
Trenched MOSFETs (6 µm-thick n⁻-GaN)

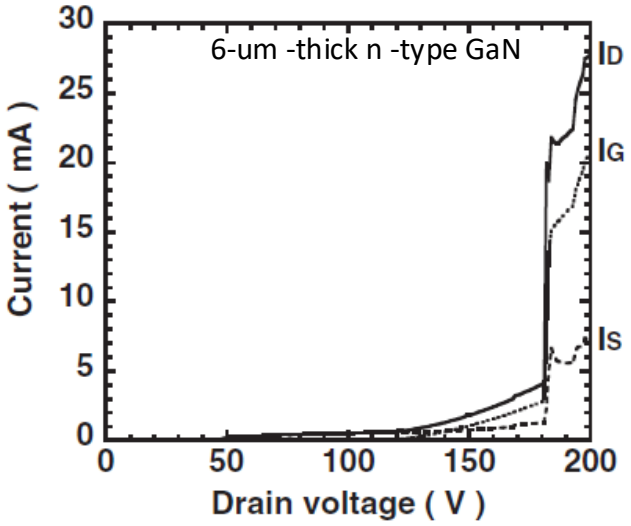


Ron = 9.3 mΩ.cm2
channel mobility: 131 cm2/(Vs)



Wet-etch (TMAH) to yield vertical sidewalls





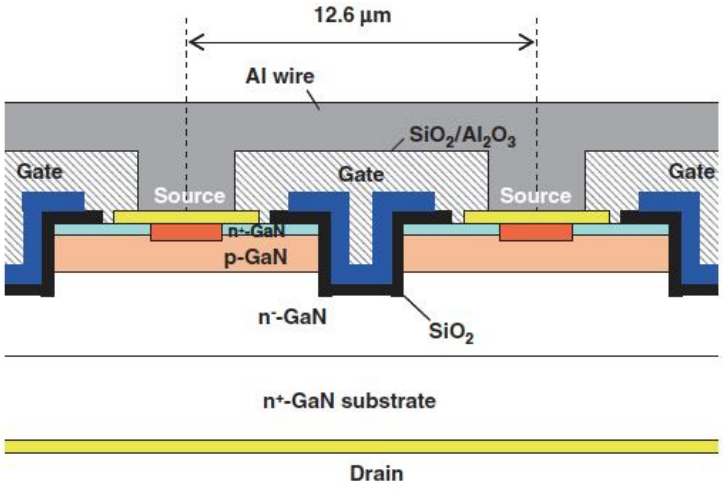
Key challenges:
Large on-resistance
Poor breakdown voltage

ROHM: H. Otake, et al., Appl. Phys. Express, 1, 011105 (2008)

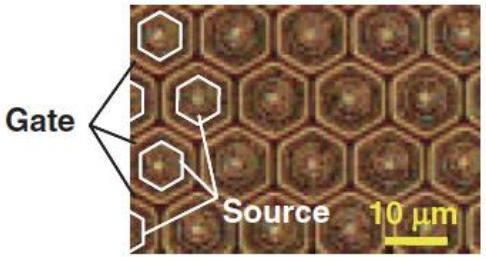
Toyota: M. Kodama, et al., Appl. Phys. Express 1, 021104 (2008)

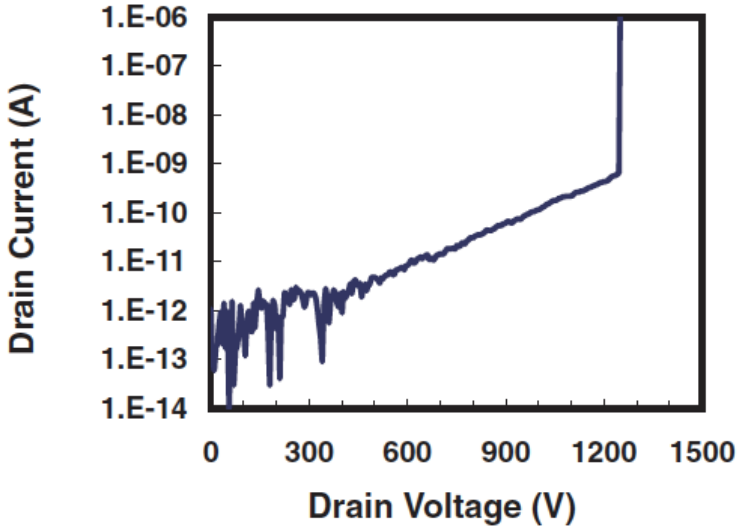
GaN vertical transistors

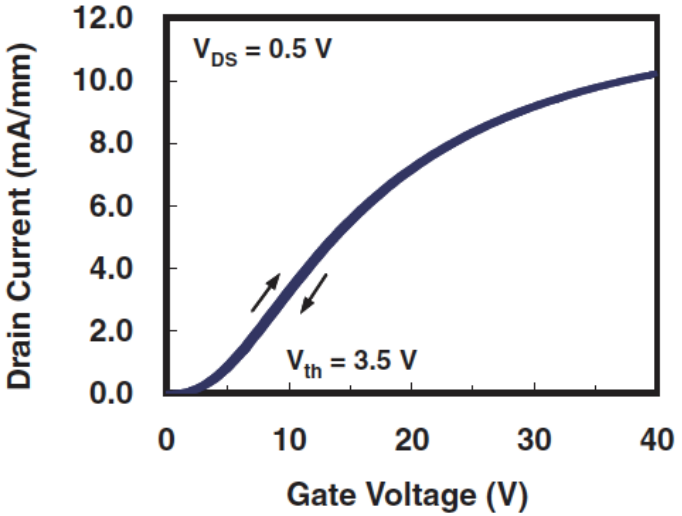
Trenched MOSFETs (13 µm-thick n^--GaN)



(a)





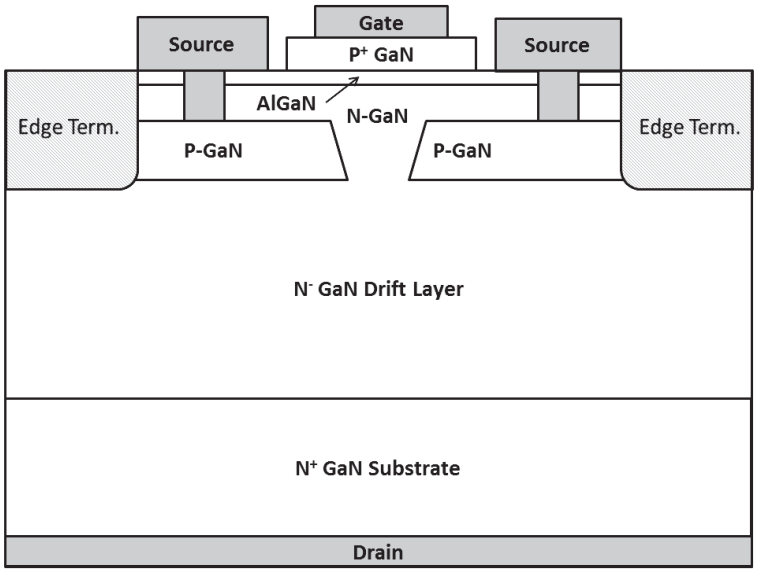


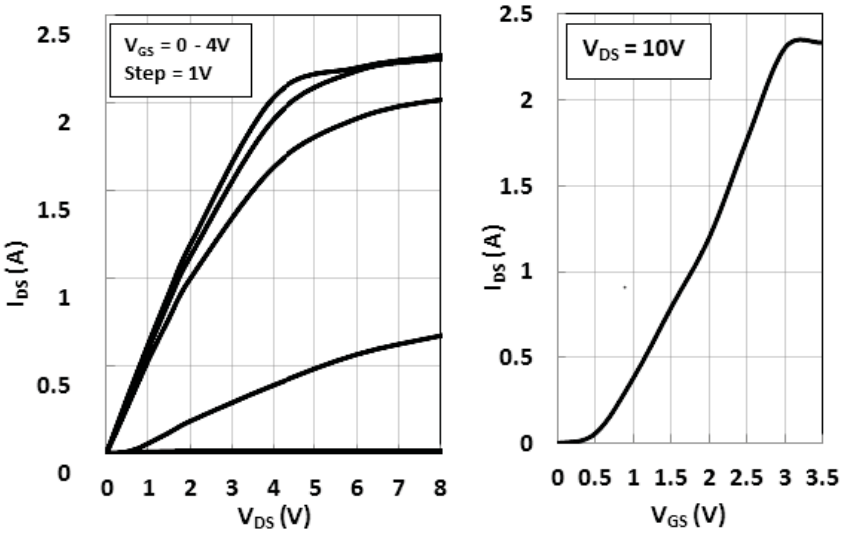
- Specific on-resistance of 1.8mΩ ·cm^2
- 1.2KV breakdown voltage
- 13-µm-thick n^--GaN
- Nd = $9x10^{15}$ cm^{-3}

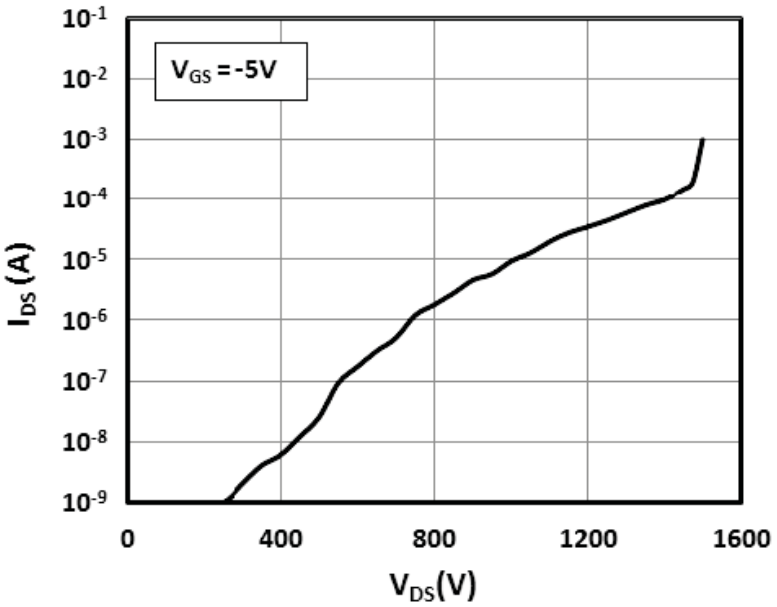
TOYODA GOSEI: T. Oka, et al., Appl. Phys. Exp., vol. 8, no. 5, p. 054101, 2015

GaN vertical transistors

Vertical devices: CAVETs







drift region net doping: ND -NA = 10^{16} cm^{-3}

drift layer thickness is 15 µm

Ron = 2.2-m-cm2

- **Doesn't rely on channel on the p-GaN**
- Normally-off behavior is difficult

UCSB: I. B. Yaacov, et al., "AlGaN/GaN current aperture vertical electron transistors with regrown channels," J. Appl. Phys., vol. 95, no. 4, pp. 2073–2078, Jan. 2004

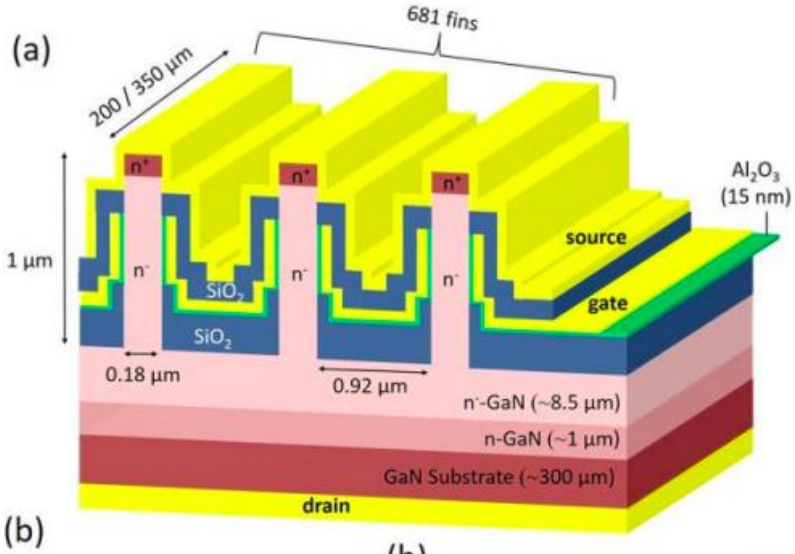
UCSB: S. Chowdhury et al., "CAVET on bulk GaN substrates achieved with MBE-regrown AlGaN/GaN layers to suppress dispersion," IEEE Electron Device Lett., vol. 33, no. 1, pp. 41–43, Jan. 2012.

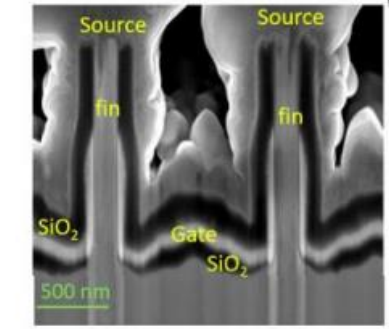
Avogy: H. Nie, et al., "1.5-kV and 2.2-m-cm2 vertical GaN transistors on bulk-GaN substrates," IEEE Electron Device Lett., vol. 35, no. 9, pp. 939–941, Sep. 2014

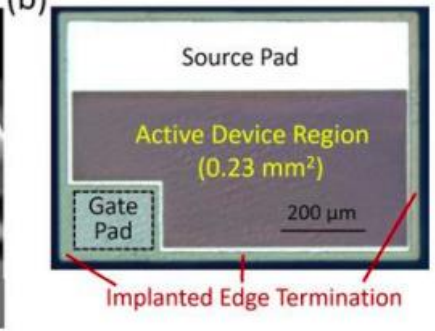
GaN vertical transistors

Vertical devices: Unipolar device

Work function difference between the gate metal and GaN depletes all electrons: enables normally-off operation.







fin width: 180 nm

threshold voltage of 1.3 V

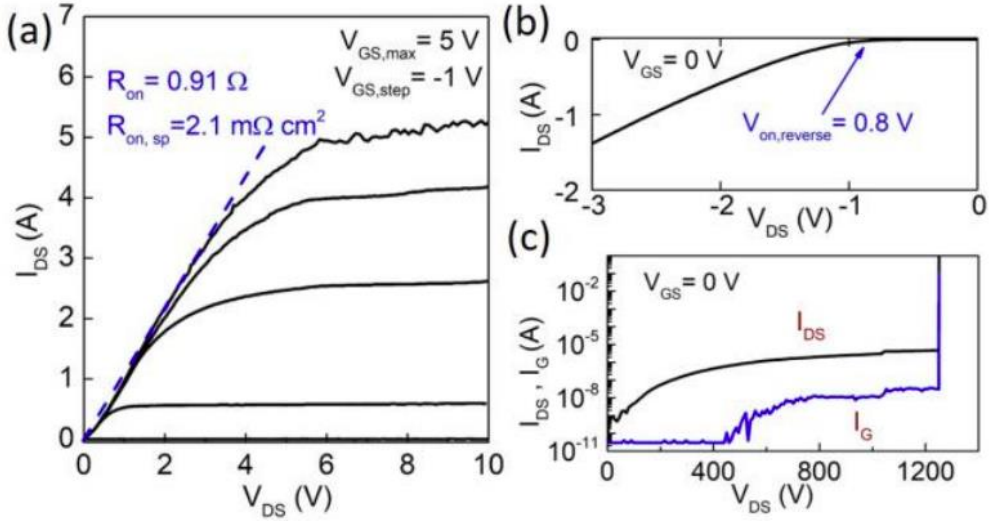


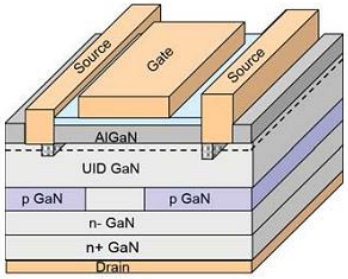
Fig. 2. (a) Device output curves and the extracted R_{on} and $R_{sp,on}$. (b) Reverse conduction curves and the extracted reverse turn-on voltage. (d) Off-state leakage characteristics at V_{GS}=0 V with a BV of 1250 V.

MIT: Y. Zhang et al. IEEE Electron Device Letters, Volume: 40 , Issue: 1 , Jan. 2019

Vertical GaN devices on Silicon substrate

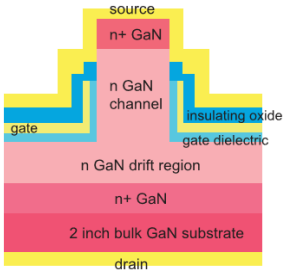
There has been a significant progress on GaN vertical devices on bulk GaN substrates:

CAVET



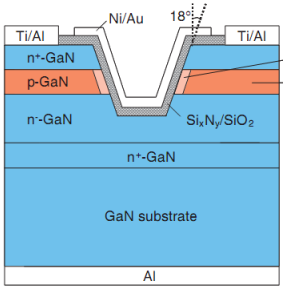
UCSB, Avogy, Toyoda, UC Davis

Fin MOSFET



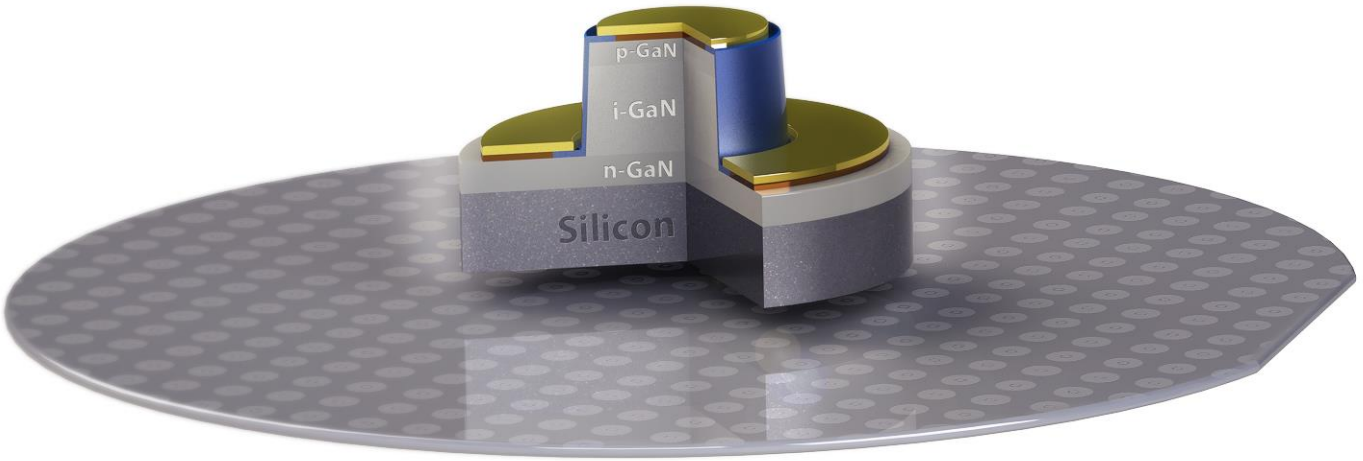
MIT

Trench MOSFET



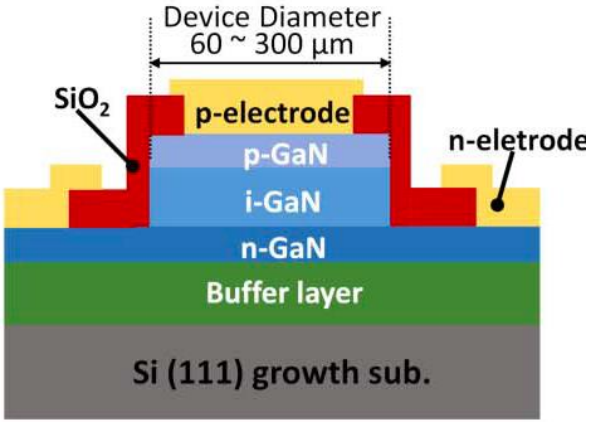
UCSB, Toyoda, ROHM

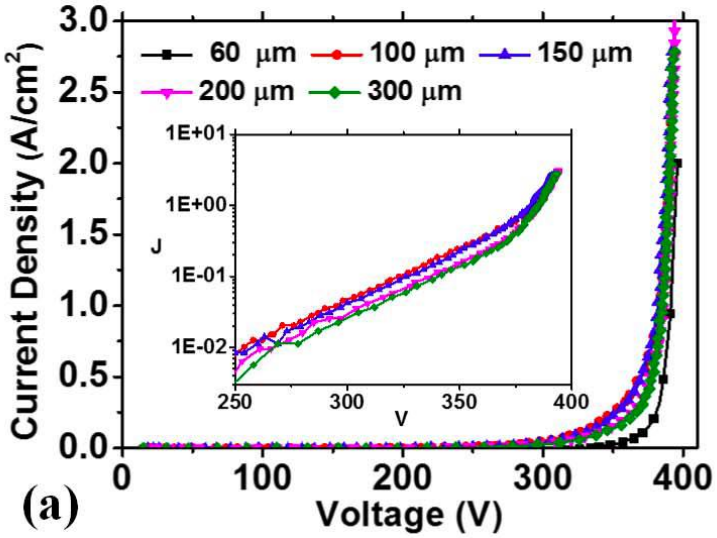
Vertical GaN-on-Silicon devices

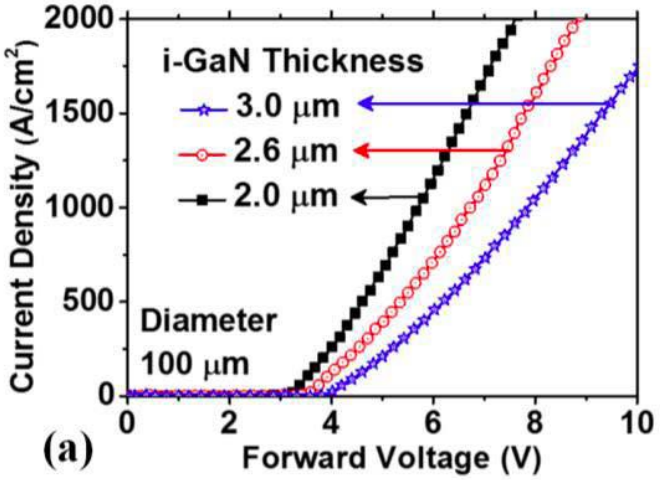


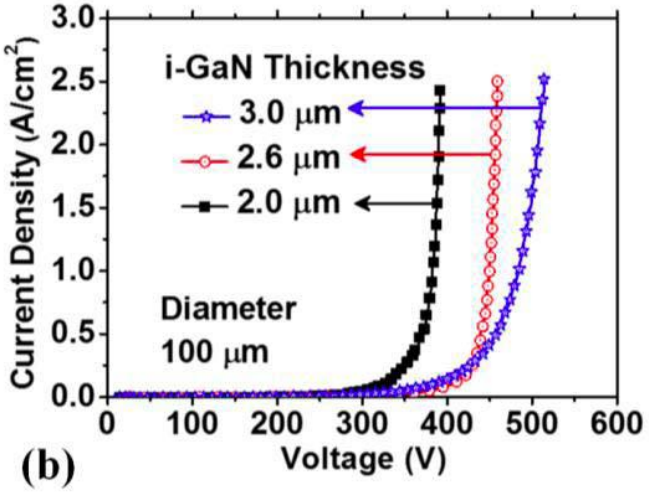
GaN Power PiN diodes

GaN PIN diodes on Silicon substrates (< 3um drift layer)







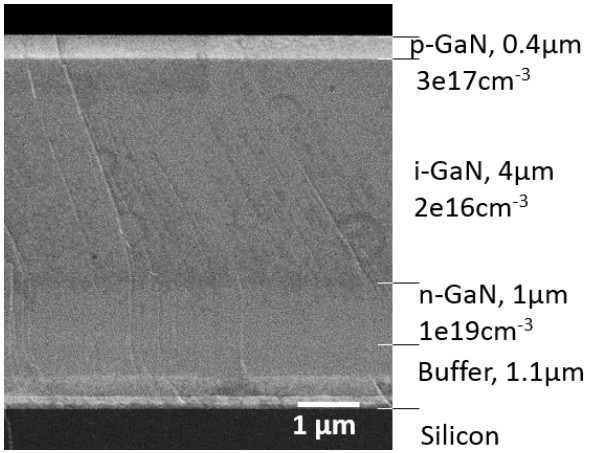


- 2-μm-thick undoped i-GaN layer
- specific on-resistance of 2.6 mohm –cm2
- breakdown voltages of 390 V

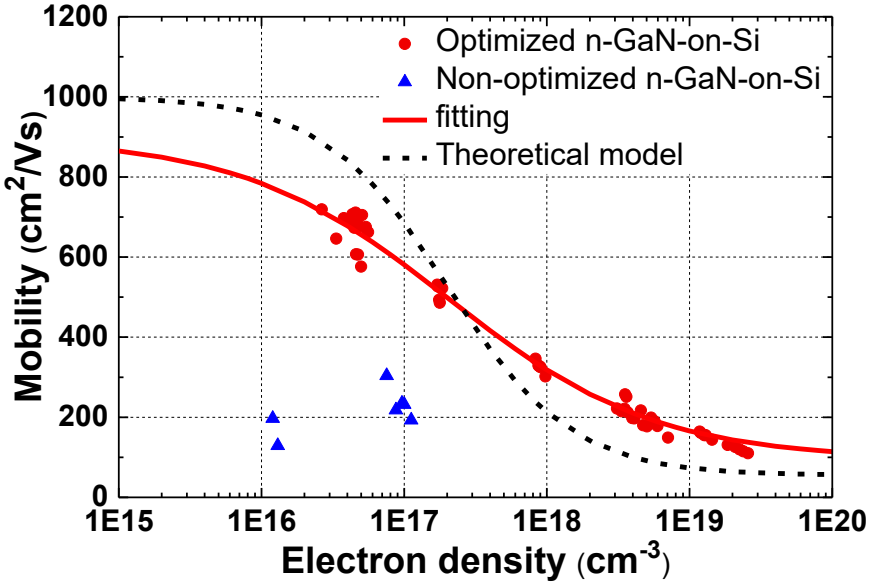
HKUST: X. Zhang, X. Zou, X. Lu, C. W. Tang, and K. M. Lau, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 64, NO. 3, MARCH 2017

First Challenge: growth of thick GaN on Si

6.5 um-thick GaN grown on 6”-silicon substrate



4 um-thick drift

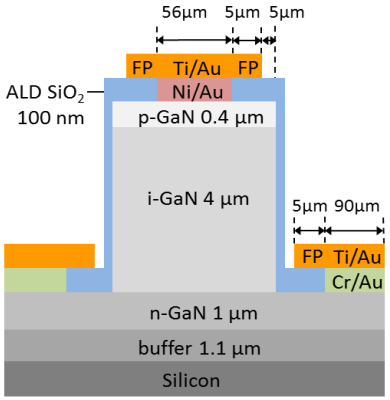


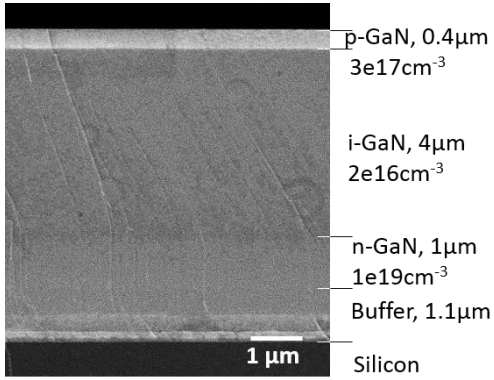
- FWHM of 235 arcsec and 307 arcsec in (002) and (102) directions
- Estimated TDD of 2.95×10^8 cm^{-2}
- Excellent mobility of 720 cm^2/Vs in UID-GaN

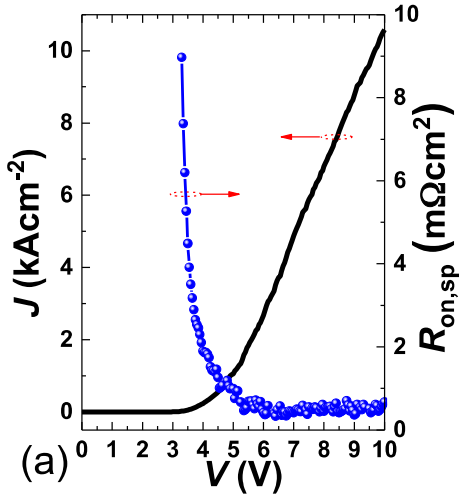
Epi structure by Dr. Kai Cheng, Enkris semiconductors

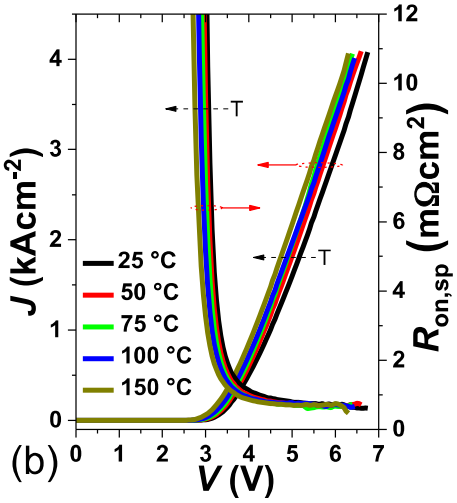
R. A. Khadar, C. Liu, L. Zhang, P. Xiang, K. Cheng, and E. Matioli, IEEE Electron Device Lett., vol. 39, no. 3, pp. 401–404, 2018

Quasi-vertical GaN-on-Si power devices



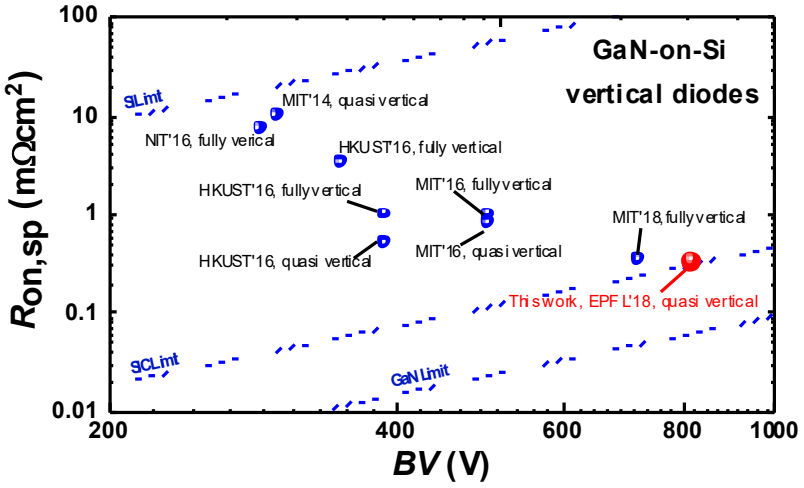




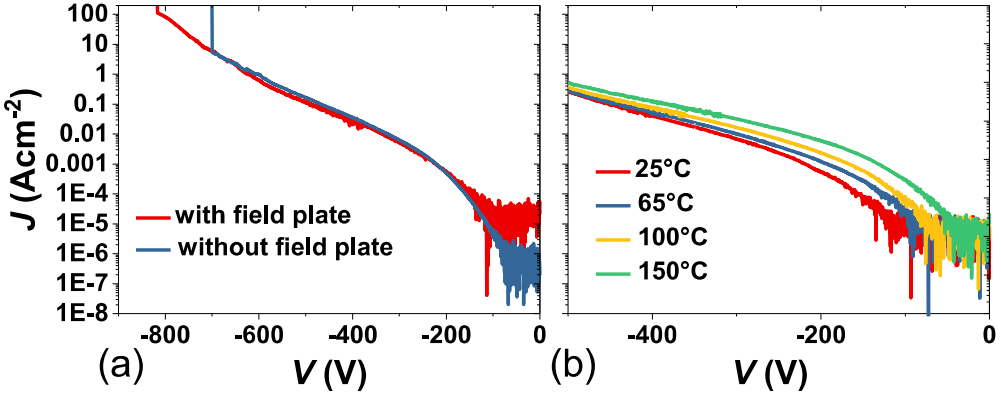


Current density over 13 kA/cm^2
Low RON 0.3 mΩcm2

Excellent mobility of 720 cm^2/Vs in UID-GaN,



High breakdown voltage of 820 V

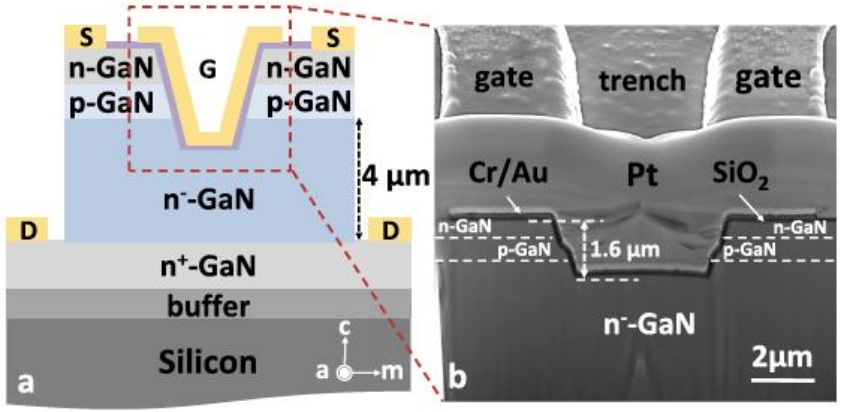


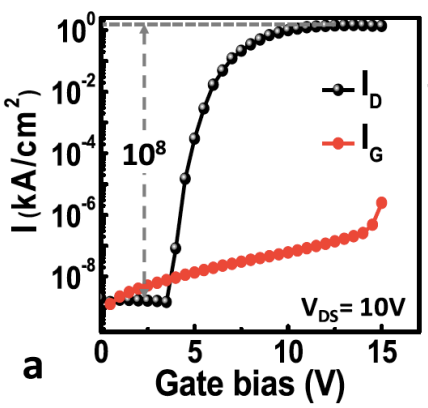
Excellent performance with a BFOM of 2.0 GW/cm^2

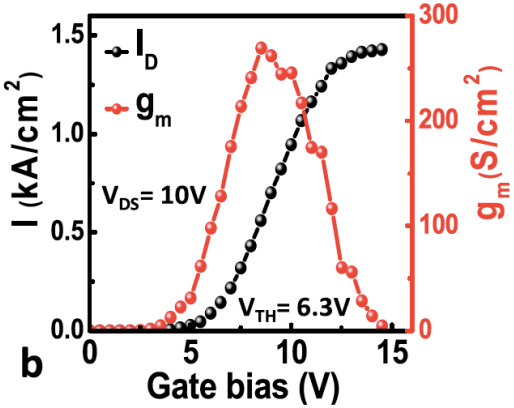
R. A. Khadar, C. Liu, L. Zhang, P. Xiang, K. Cheng and E. Matioli, ***IEEE Electron Device Letters***, Feb. 2018.

Quasi-vertical power devices

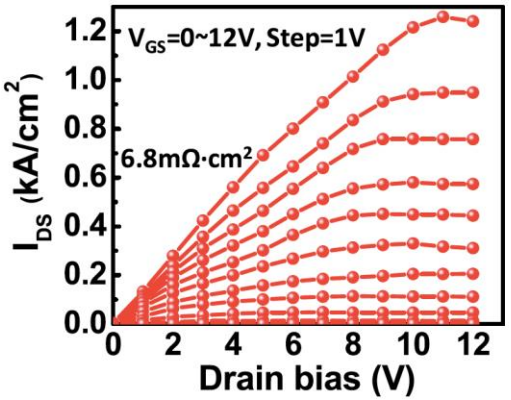
How about **vertical GaN power transistors** on cost-effective Silicon substrates:

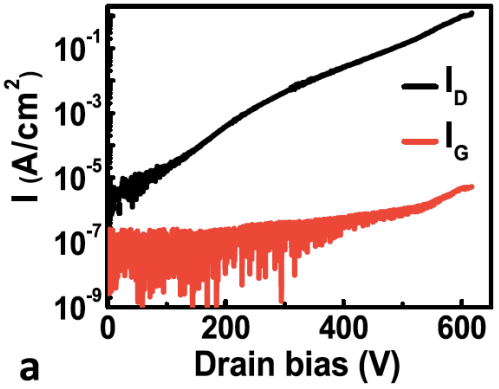






High breakdown voltage of 645 V





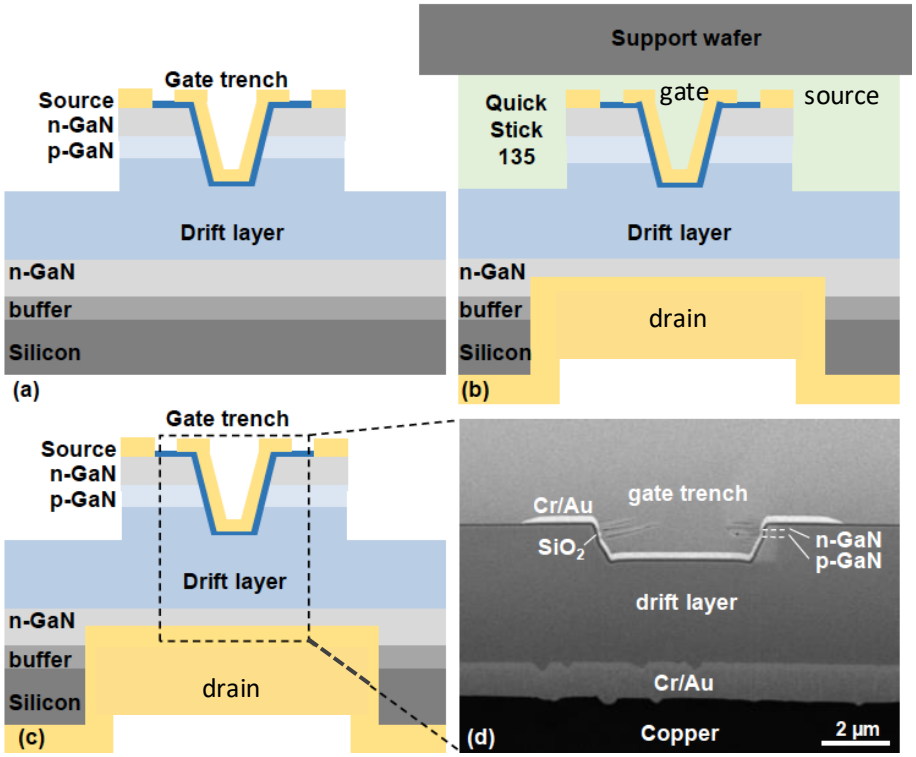
Large on-resistance:

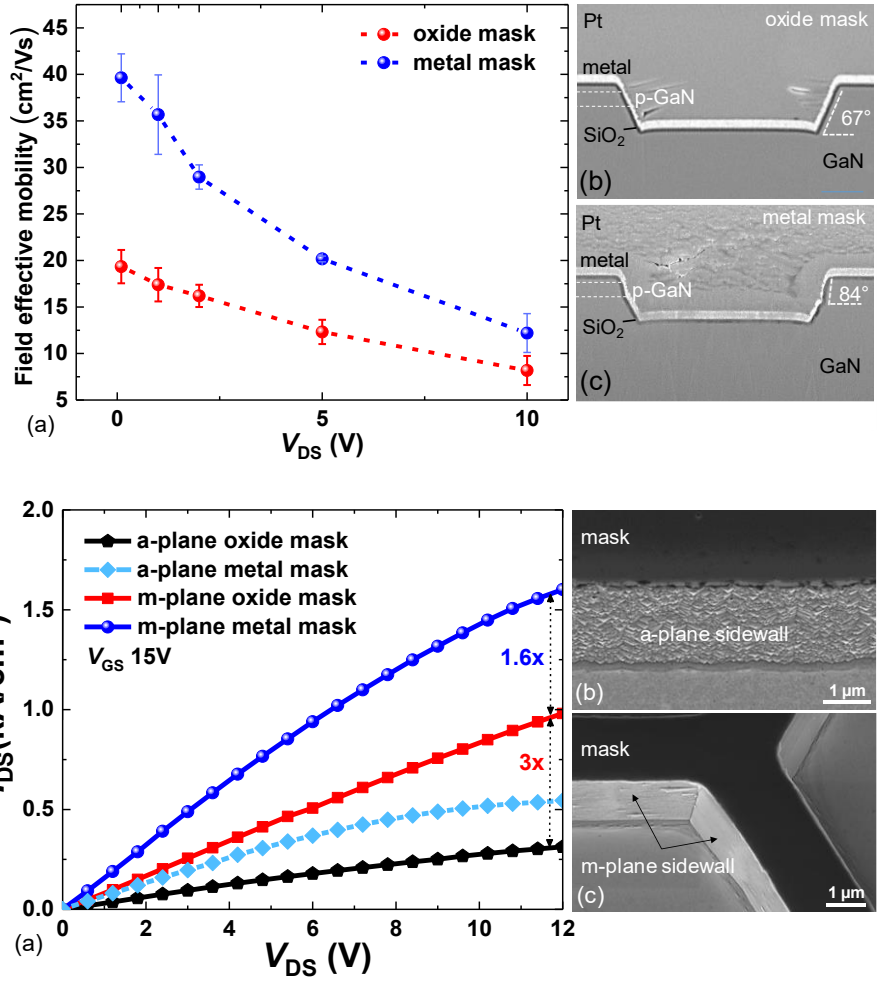
- Poor channel mobility of 17.8 cm2/V.s
- Quasi-vertical: current crowding at n-GaN layer

C. Liu, R. A. Khadar, E. Matioli, **IEEE Electron Device Letters** 39 (1), 71-74, Jan. 2018

First fully-vertical power transistors on Silicon

Demonstration of fully **vertical GaN power transistors** on cost-effective 6” Silicon

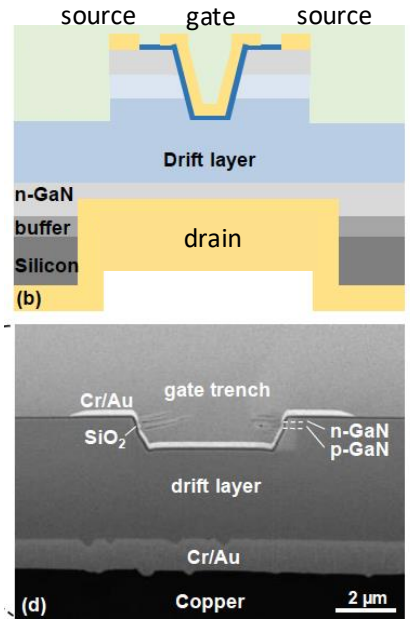


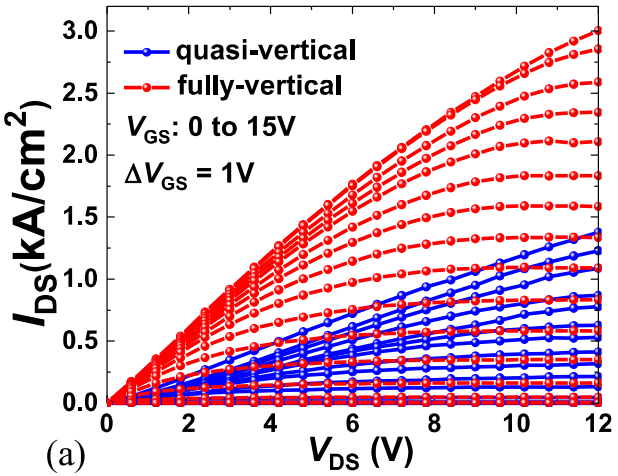


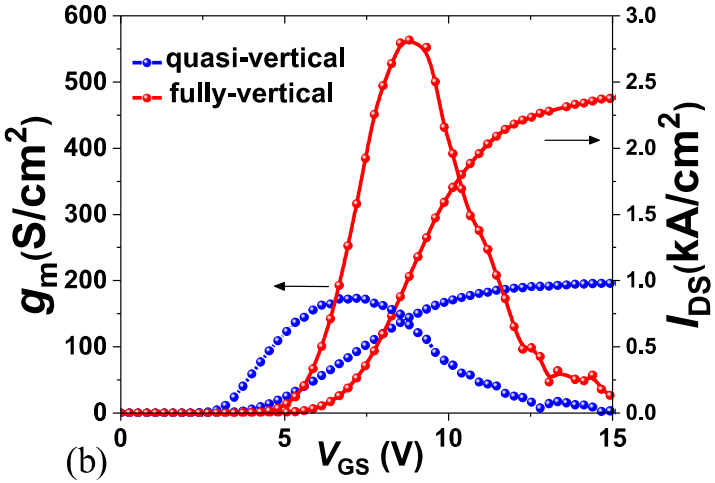
R. A. Khadar, C. Liu, R. Soleimanzadeh, E. Matioli, **IEEE Electron Device Letters**, vol. 40 , Issue: 3 , **Jan 2019**

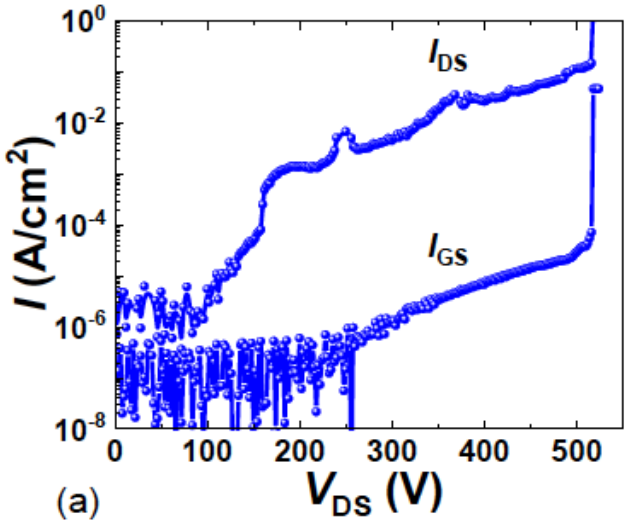
Fully-Vertical power transistors

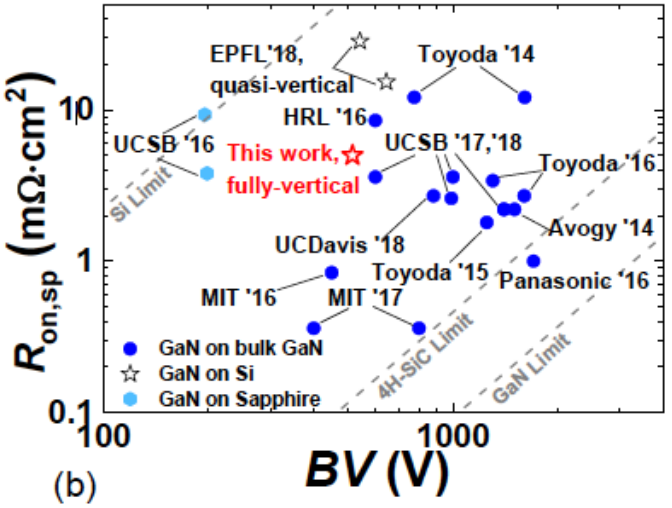
First demonstration of fully **vertical GaN power transistors** on cost-effective Silicon









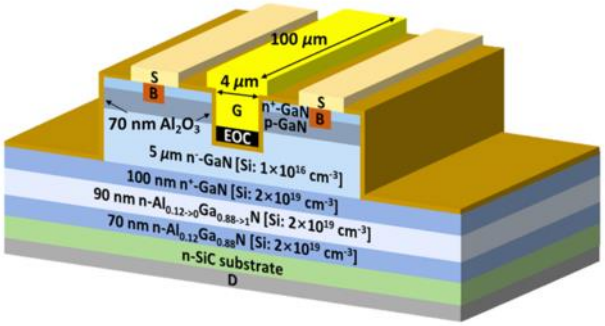


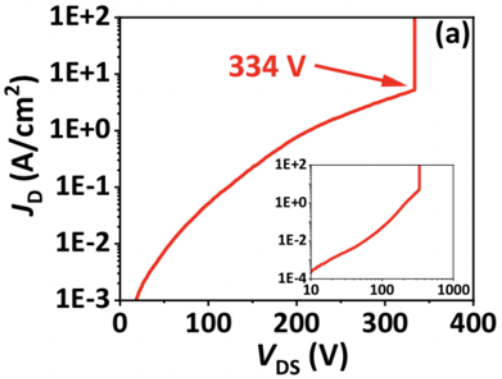
Major step toward high-performance GaN vertical power transistors on low-cost silicon substrates

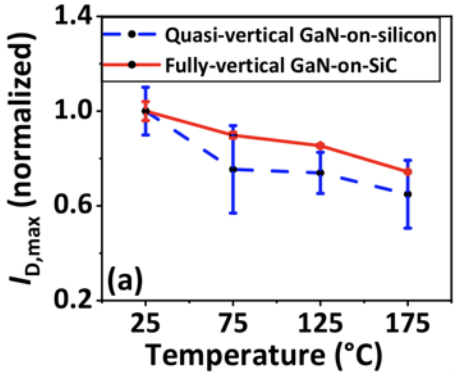
R. A. Khadar, C. Liu, R. Soleimanzadeh, E. Matioli, **IEEE Electron Device Letters**, vol. 40 , Issue: 3 , **Jan 2019**

Fully-Vertical power transistors on SiC substrates

- **Trench MOSFET**

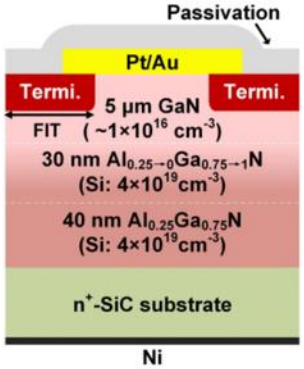


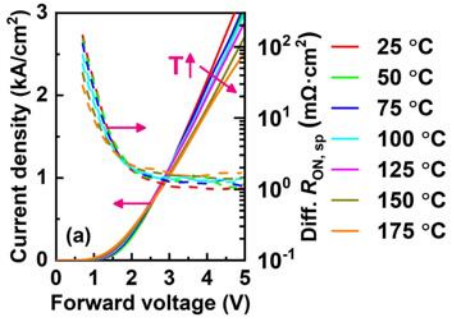


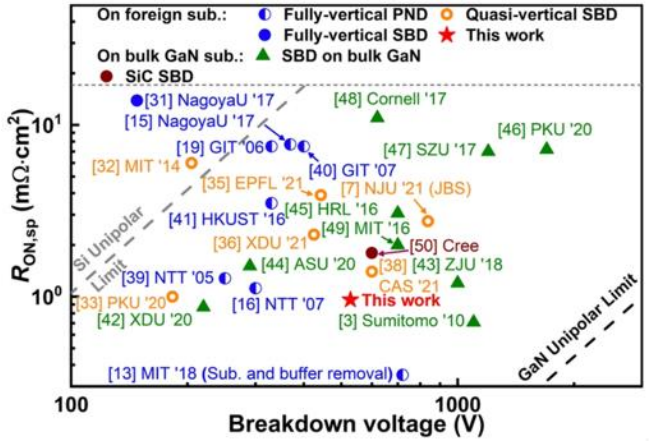


J. Li et al. ***IEEE Electron Device Letters*** *(2024).*

- **Schottky diode**







Y. Li et al. ***IEEE Transactions on Electron Devices*** *70.2 (2022): 619-626.*

New concept:

Field management using polarization engineering

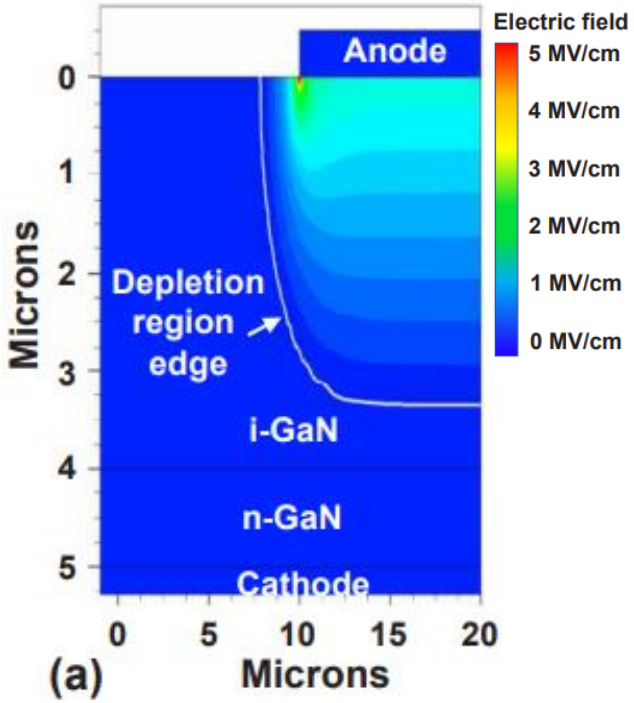
Can we use a low band-gap material for higher voltage devices?

Motivation: electric field management

Schottky Barrier Diode (SBD)

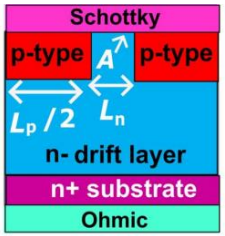
High E at Schottky interface

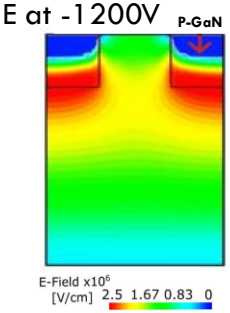
High reverse leakage current



R. A. Khadar *et al.*, ISPSD, pp. 147-150 (2021)

Junction Barrier Schottky (JBS)

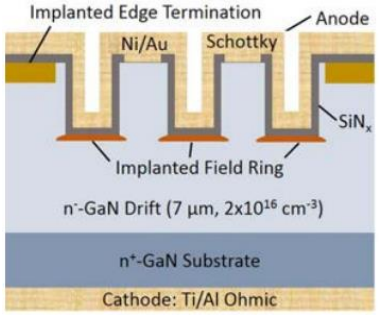


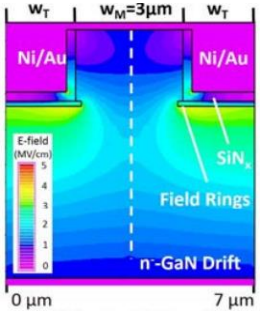


Inevitable R_{on} increase

M. Matys *et al.*, Jpn. J. Appl. Phys. 62, SN0801 (2023)

Trench MOS Barrier Schottky (TMBS)





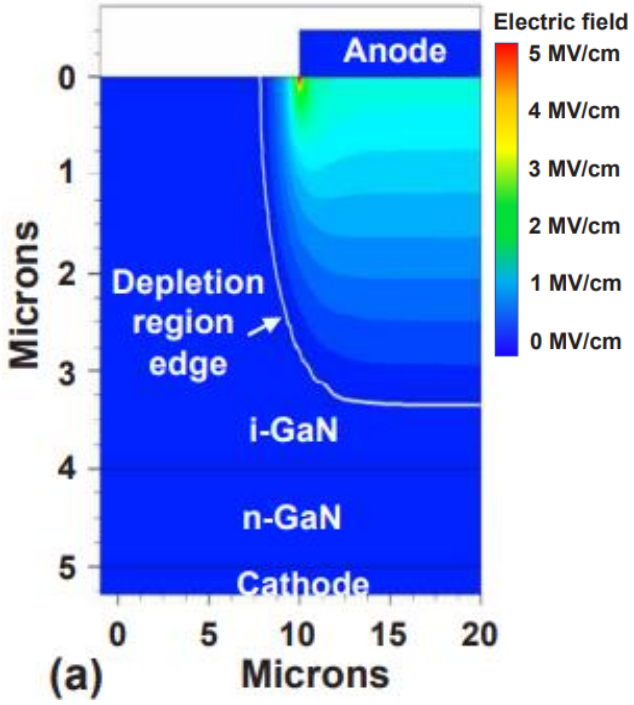
Careful design/complex fabrication process

Y. Zhang *et al.*, IEDM, pp. 10.2.1-10.2.4 (2016)

Motivation: electric field management

Schottky Barrier Diode (SBD)

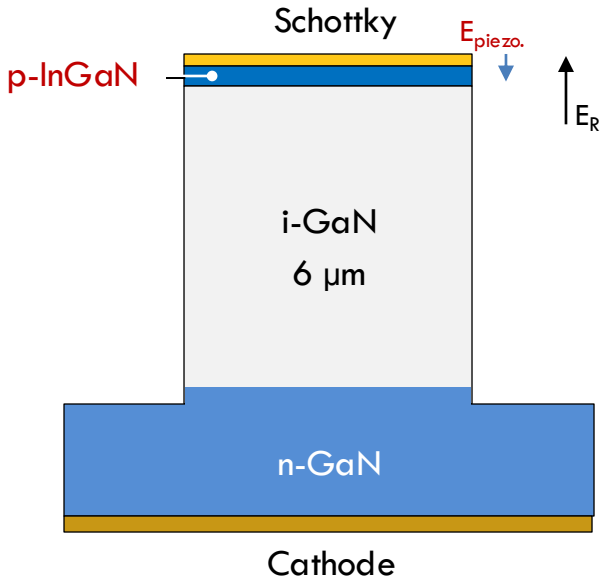
High E at Schottky interface
High reverse leakage current



R. A. Khadar *et al.*, ISPSD, pp. 147-150 (2021)

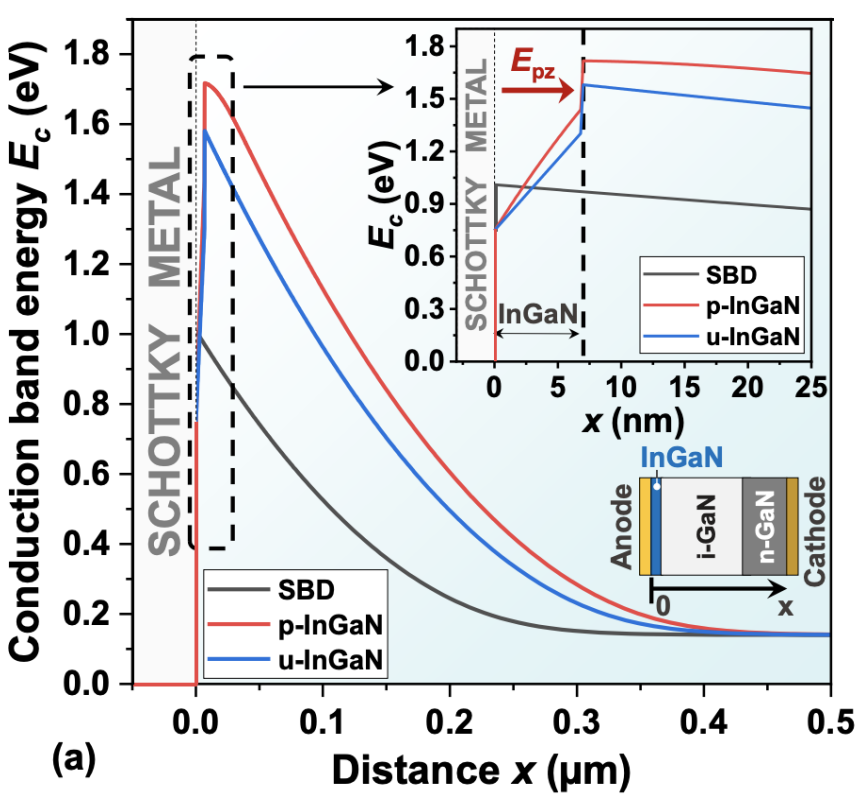
Our approach:

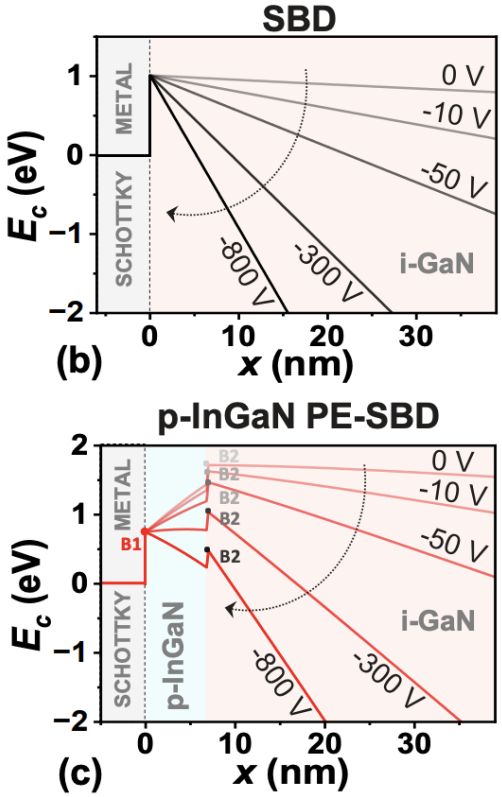
Polarization fields of InGaN for field management



Can we use a low band-gap material for higher voltage devices?

Polarization fields of InGaN for field management





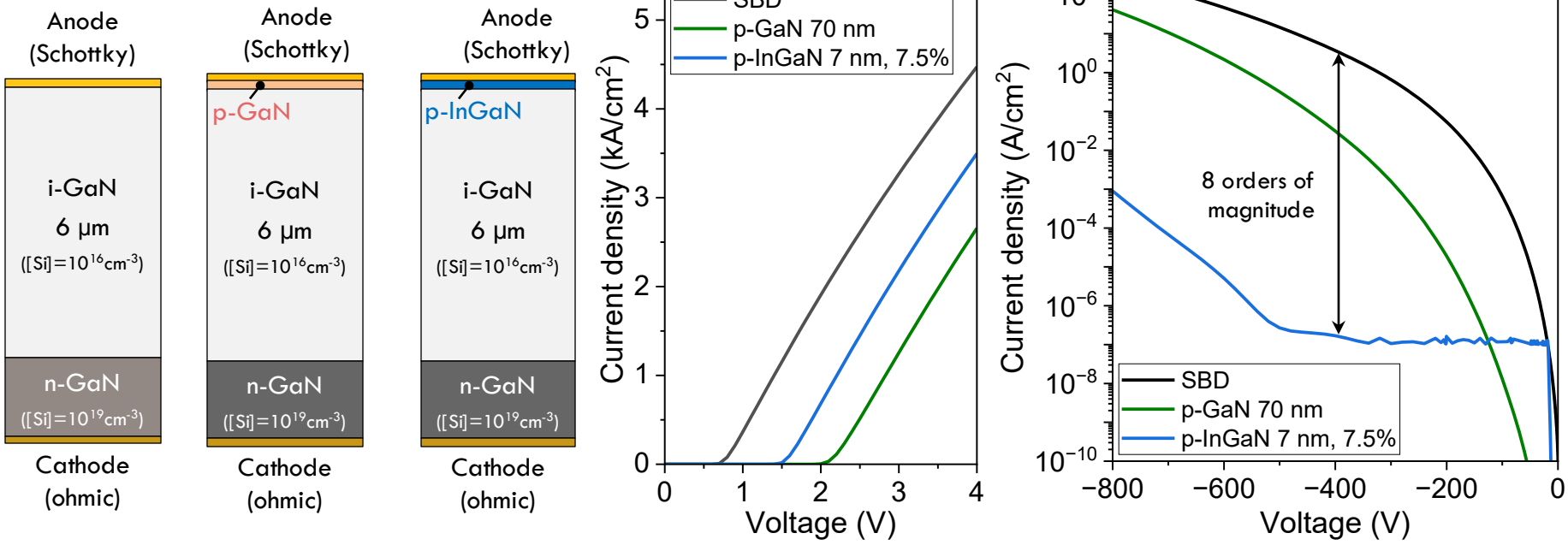
At -800 V:
E_{max} = 1.94 MV/cm

At -800 V:
$E_{max,\ p\text{-}InGaN}$ = 0.9 MV/cm

Piezoelectric field (+) in p-InGaN opposes external reverse electric field (-)

A. Floriduz, Z. Hao and E. Matioli, **IEEE Electron Device Letters 2024** (online access)

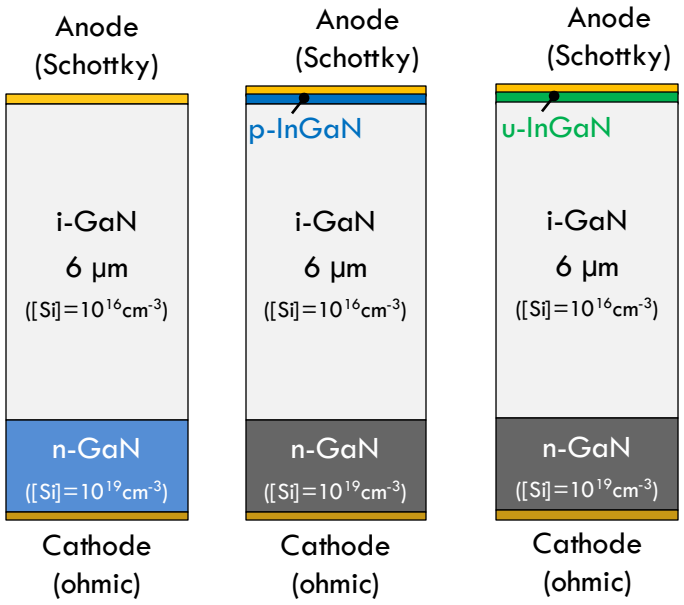
TCAD simulations: thin p-InGaN layer

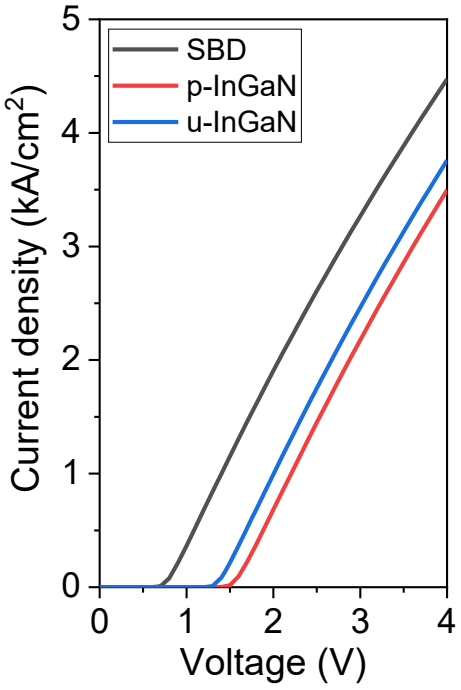


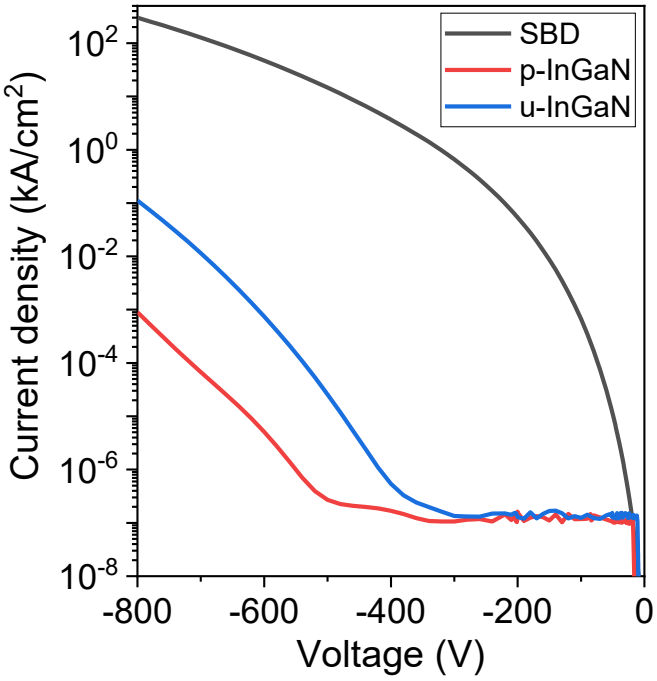
Large decrease in leakage current using thin p-InGaN

A. Floriduz, Z. Hao and E. Matioli, **IEEE Electron Device Letters 2024** (online access)

TCAD simulations: p-InGaN vs. uid-InGaN



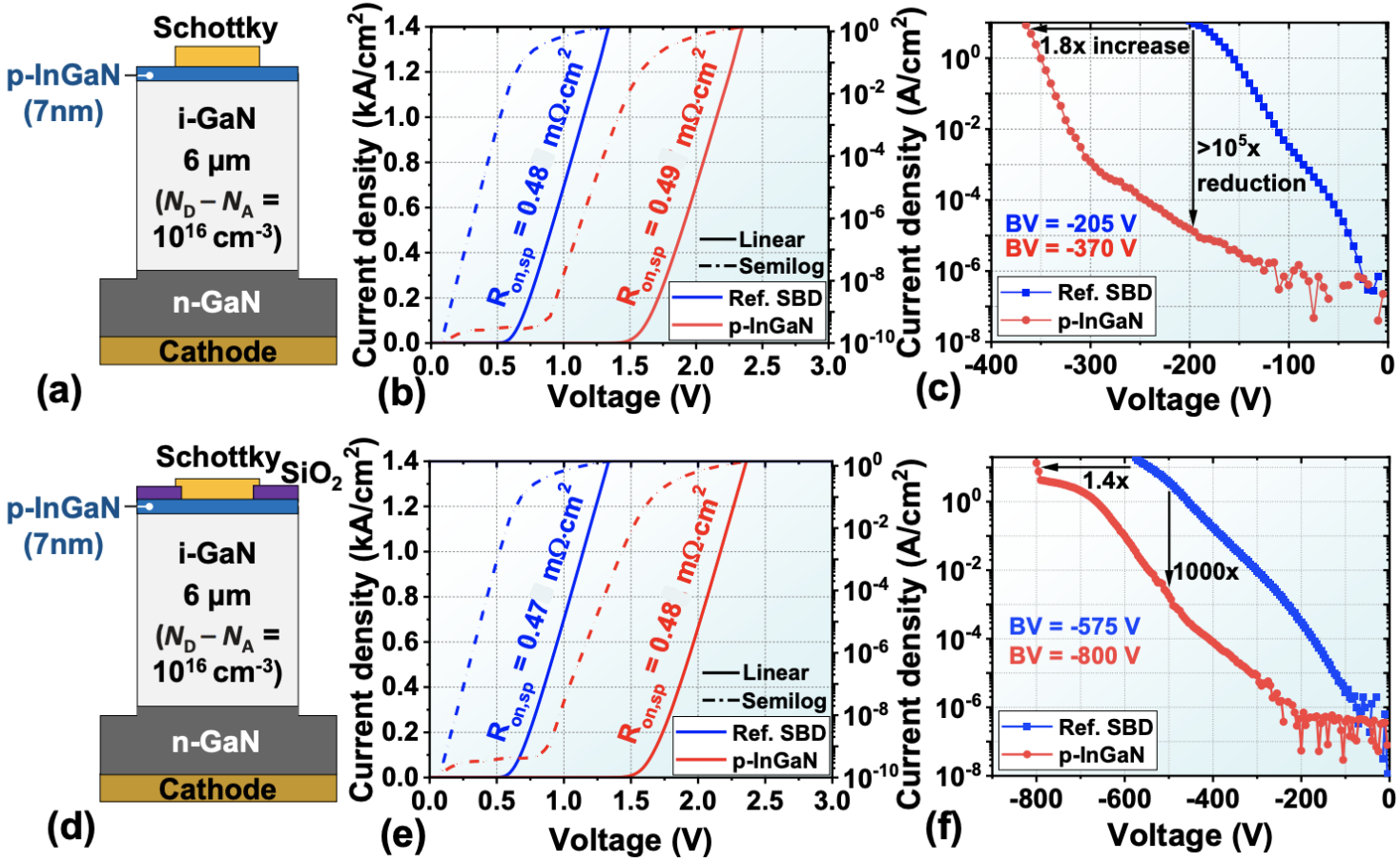




InGaN 7 nm, [In] = 7.5%

Piezoelectric polarization of InGaN:
Dominant contribution to electrical performances

p-InGaN/GaN SBDs with High BV with low RON

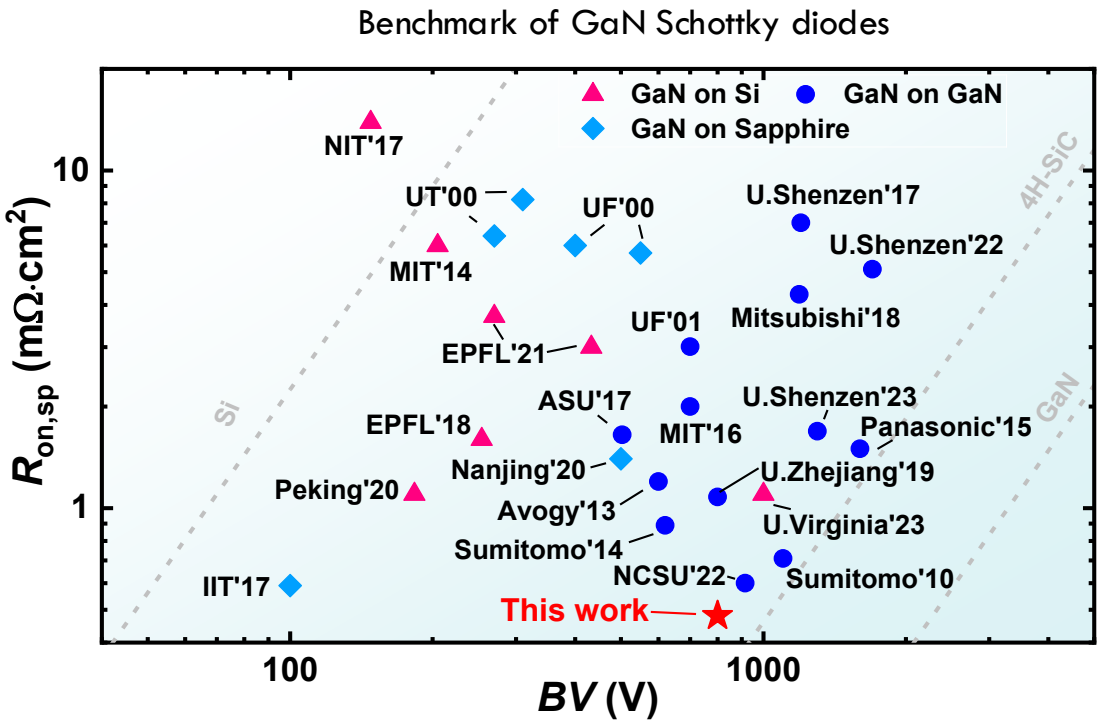


R_{ON}: 0.48mΩcm^2
BV: 800 V

Low band-gap InGaN for larger voltage devices

A. Floriduz, Z. Hao and E. Matioli, **IEEE Electron Device Letters 2024** (online access)

High Baliga Figure-of-Merits (BFOM)



High Baliga Figure-of-Merit (BFOM) = 1.32 GW/cm^2

Conclusions

Vertical power devices on bulk GaN:

- Excellent performance near the GaN limits with text-book like features

Future challenges:

- Substrate too expensive and too small
- Localized doping: can we use ion implantion effectively in GaN?
- Improved Mg-doping: low activation of Mg dopants leads to poor transport in the channel

Vertical GaN-on-Si power devices:

- Relatively thick GaN layers on Silicon
- Quasi-vertical PiN diodes and MOSFETs
- First demonstration of fully-vertical GaN-on-Si MOSFET

Future challenges:

- Growth of thicker drift GaN layers
- Reduction of dislocation density

Low band-gap InGaN for larger voltage devices